EDA & Testing

PE01

AN-HRNS: AN-Coded Hierarchical Residue Number System for Neural Network Acceleration and Reliability

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Residue Number Systems (RNS) can simultaneously improve computing acceleration, area reduction and power saving. For reliability-critical applications, disjoint modularization empowers the redundant RNS fault tolerance. However, parallel multiple modular redundancy takes a huge number of converters. In this paper we develop a hierarchical RNS and apply the AN-codes for both sub-RNS error correction and MMR checking. An expanded residue-to-binary converter is developed for highly reduction of the whole multiple-module redundancy decoder. This is the first paper to incorporate AN codes to the RRNS applied in highly-reliable neural networks. From experimental results, only one extra redundant modulus is required. The g=(k+2)(k+1)/2 residue-to-binary converters and g(g-1)/2 comparators can be reduced to only k+1 decoders. From BLER simulations, more than 126 times of MTBF can be achieved.

PE02

Impact of Humidity on ESD Robustness of Integrated Circuits and Systems

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Nowadays the electronic devices may be used everywhere with extreme environment, including very high or low humidity. The effects of humidity on the electrostatic discharge (ESD) robustness of the electronic devices are needed to be studied. In this work, the simple integrated circuits and systems to simulate the electronic devices with various humidity are studied. The impact of the humidity on ESD robustness are found and studied in this paper.

PE03

Efficient Yield Analysis for SRAM-Based System with PDF Consolidation Methodology

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SRAM-based system is one of the most popular design in various applications. However, the high yield request of SRAM system brings difficulties to verification tasks due to high simulation cost for yield estimation. Importance sampling techniques are able to reduce the number of samples in high sigma analysis. However, the complexity is still high if the entire memory system with peripheral circuits are simulated together. To handle this issue, we propose an efficient yield analysis method for the overall SRAM system. Instead of analyzing whole system directly, the proposed methodology evaluating each circuit block first. Then, the interactions of circuit blocks are considered to evaluate the accurate system performance with the prior distribution of each block. In this way, the overall accurate design yield can be obtained easily. The experimental results show that the proposed methodology is able to estimate the design yield of rare failure SRAM designs efficiently with high accuracy.

PE04

Dynamic Power Model for SRAM-Based In-Memory Computing

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Because the demand for low-power equipment is growing up, extending battery life and reducing heat dissipation become important considerations. In recent years, In-Memory Computing (IMC) technology is proposed to solve the bottleneck of data movement in AI edge designs. In order to implement simple computation, the IMC designs often adopt analog operations, which bring new issues to power estimation. Because the complexity of power estimation at transistor-level is often too high for large design, this work proposes a high-level power consumption model to provide different power values for different input patterns. We focus on the effect of switched data bits because it will directly cause current change. Therefore, we propose an efficient approach to record the power consumption with different Hamming distance. As shown in the experimental results, the proposed power model is able to reduce the power estimation time for IMC designs and still retains similar result under different input patterns.

PE05

Aging-aware Computing In-memory Technique for 8T SRAM Multi-bit Dot Product Engine

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Von Neumann architecture which separates the computing logic and the storage area has been considered as the fundamental architecture of nearly all digital computers nowadays. The data intensive applications such as image recognition or cryptography may transfer large amount of data between memory and the computing cores, which causes a well-known von Neumann bottleneck due to the limitation of communication bandwidth. Computing In-Memory (CIM), which directly perform in-situ operations at memory, has been considered as one of the promising solutions to overcome von Neumann bottleneck. Previous researchers have proposed an 8T-SRAM-based CIM architecture to perform multi-bit dot product computations by analog charging/discharging operations. However, such operations are very sensitive to variations as well as aging effects such as Bias Temperature Instability (BTI) and/or Hot Carrier Injection (HCI). To provide a reliable CIM multi-bit dot product engine, in this paper we propose an aging-aware in-memory computing framework which consists of an aging detection method and an aging tolerance technique. Specifically, we apply Dynamic Voltage Frequency Scaling (DVFS) on CIM structure to compensate the current drop due to variations and aging effects. Experimental results show that we can double the lifetime of CIM structure with 1.185x extra power consumption in average.

PE06

2DAN-BNN: Two-Dimensional Error Location for AN-Code Decoders in Binarized Neural Networks

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AI accelerator, binarized neural network (BNN) becomes the low-cost high-accelerated inference machine for consumer electronics. However, except acceleration, power dissipation, area cost and reliability are also critical issues of AI accelerators. In safety-critical applications, the reliability issue becomes hard to trade and even more critical than cost and acceleration. Recently, people are understanding that only arithmetic codes can correct errors online. AN codes are effective and efficient arithmetic codes for improving the reliability of a BNN, but each class output requires an AN decoder. As a result, the power dissipation and associated area overhead not only highly in-crease the cost but also seriously affect the performance. In this paper, we propose a two-dimensional error-locating technique for sharing only a decoder. From experimental results, more than 97% of the logic elements and the associate power dissipation can be reduced.

PE07

Reliable Advanced Encryption Standard System Design with PUF-based Key Generators

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Hardware Trojans and side channel attacks have become serious threats for modern cryptoprocessors. One of the attacker's goals is stealing key information for encryption and decryption algorithms. Therefore, it is important to find robust techniques to protect the key information. With the properties of robust, unique, easy to evaluate, difficult to replicate, and very difficult or impossible to predict, it has been shown that Physically Unclonable Function (PUF) is a promising cryptographic primitive to be a key generator. In this paper, we propose a reliable Advanced Encryption Standard (AES) system which applies Arbiter PUF (APUF) and Ring-Oscillator PUF (ROPUF) as key generators. We implement our AES system with PUFs on different FPGAs, and demonstrate the effectiveness of different PUF designs as key generators to protect the encryption circuit and decryption circuit of AES system. Moreover, we carefully study how the different place-and-route settings on FPGA influence the PUF behavior. Finally, we show the resource utilization and power analysis results on Xilinx Zynq-7000 SoC ZC702. Experimental show that our design not only can successfully provide reliable key to AES but also introduce acceptable design overhead.

PE08

A Systematic Region-Based Interleaving Reduction Approach for Concurrent Bug Testing

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In this paper, we propose an effective concurrency bug testing approach that focuses on suspicious bug-causing code regions instead of indiscriminately testing the whole program. Additionally, with a simple loop heuristic, the region-based approach effectively avoids the state-explosion problem. It is highly efficient while guaranteeing to find any existing concurrency bugs in the specified code regions. We also devise an optimization scheme to reduce the number of interleavings to be examined to achieve maximum efficiency. Our method can conveniently identify bug-causing interleavings and hence significantly improve debugging efficiency. We have implemented the proposed approach and successfully tested on a few large application cases. The experimental results show that the approach can precisely identify bug sources and perform much more effectively than traditional approaches.

PE11

Exploring All Pairs of Circuit Nodes to Generate Combinational Hardware Trojan Detecting Patterns

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Hardware Trojan (HT) invasion has become an important issue in the rapidly changing semiconductor field. In this paper, we propose a method to explore all possible pairs of circuit nodes and generate all required test patterns for detecting assumed combinational HT designs. Comparing to original stuck-at fault (SAF) patterns, we add only 1 to 8 multiples of additional patterns because of using pattern compression. These patterns can be prepared in very short time. In addition, experimenting on detecting those HT not assumed by our methods, we find that our patterns can have 43X stronger detectability than SAF patterns for the benchmark circuit s38584.

PE12

Applying Machine Learning to Custom-fix Timing Violations after Routing

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Timing aversion is a challenge in the physical design flow. However, timing analysis can only be performed accurately after the routing is completed, and in the process of fixing timing violations, the physical design tool can automatically converge most of the timing violations, but there are still some problems require a lot of time and cost for engineers to fix them. Therefore, our approach uses machine learning technology to extract the features of each critical path from the database in the post-route stage, and then conducts training to quickly repair the timing violation by the developed repair scheme.

PE13

PCB Component Copper Landing Pad Design Optimization

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As the density of electronic components increases in modern PCB designs, the adjustment of copper landing pads has become a complex and essential issue during PCB layout design stage. Common copper landing pad adjusting strategies are optimized by experienced PCB layout engineers. However, manual designs are error-prone and may suffer reliability degradation. In this paper, we propose an optimization framework to legalize copper landing pads via pad offset, pad cutting, and pad shrinking operations. The experimental results demonstrate the effectiveness to significantly reduce the manual task of PCB layout engineers for time and effort saving.

PE14

Recognizing Wafer Defects by Using Statistic Analysis of Geometric Features

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This paper proposes a method for judging defects on a wafer. We first analyze the five geometric parameters of defects on wafer bin maps. We statistically obtain the parameter intervals of various wafer defects. These intervals are used to analyze unknown wafer bin maps to determine possible wafer defects. Experiments show that our feature parameter intervals are accurate for judging wafer defects, which will help construct automatic wafer defect analysis system in the future.