Poster Session

Analog & RF

PA01

A CMOS Algae Growth Period to Duty Cycle Converter for Monitoring Algae Growth Status Applications

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A CMOS algae growth period converter is newly used for applications of monitoring algae growth status. The proposed converter can transform algae growth period into duty cycle linearly. Through the duty cycle of this converter, the algae growth status could be easily and quickly obtained. A wide rail-to-rail voltage to current converter and the adjustment sensitivity circuits are designed to be adaptively used in different kinds of algae growth environment. The wide-range differential voltage is -1.5 to 1.5 V, the corresponding range of output duty cycle was 1.46 to 98.4643 %. The various sensitivities of the proposed converter were 23.496, 27.378, 32.804, and 41.209%/V. The proposed chip could be used for monitoring algae growth status applications.

PA02

A Temperature Compensation Method for Potentiometric Biosensors Based on Arrayed RuO2 Ascorbic Acid Sensing Thin Film

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The temperature effect is analyzed for the ascorbic acid (AA) biosensor based on enzymatic ascorbate oxidase (AO). To reduce this non-ideal effect, a novel temperature compensation circuit was implemented by TSMC 180nm CMOS process. By applying the proposed circuit, the temperature coefficients (TCs) with five concentrations of AA were suppressed below 201 μV/°C. The TC of the normal level of AA (0.0312 mM) in the human body was 188 μV/°C, in the temperature range from 25°C to 55°C. At present, the experiments were still in the stage of in vitro measurement.

PA03

A CMOS with Auto-High Background Immunity Position-Sensitive Detector (PSD) for High Background Light Environment

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In this paper, a CMOS with auto-high background immunity position-sensitive detector (PSD) is newly used for high background light environment. The proposed approach can successfully solve the impact of high background light on PSD. As proven by simulations, if the problem of high background light on PSD in real environment is not solved, the maximum linear error of the PSD will be over 45.25% when the intensity of background light becomes higher than 5 nA. After performing the proposed auto-high background immunity circuits, the maximum linear error can be reduced to below 1% while the intensity of background light is 40 nA. The proposed PSD could be used for high background light environment.

PA04

A Low-Temperature Variation Reference Current Source with Digital Counting Auto-Calibration Scheme

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This paper designs a reference current source that can automatically correct without being affected by temperature. It could be applied to an operational amplifier in analog-to-digital converters (ADC) to provide a stable bias condition. With a supply voltage-independent current reference, the reference current is employed in the current-controlled oscillator (CCO) to generate a clock signal depending on the current. Further, the clock compares with the reference signal provided by the quartz crystal oscillator for frequency detecting. The binary search algorithm determines the reference current by oscillating frequency change caused by the environmental deviation. The design environment of this circuit operates under the conditions of 1.8V supply voltage and -100°C to +200°C of the temperature range in using the UMC 0.18um CMOS process. Thus, it would achieve a self-healing reference current source with the low-temperature variation used in space environments.

PA05

A Charge-mode Neural Stimulator with Active Charge Balancing for Electrical Stimulation Applications

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Energy efficiency and the problem of safety are two major concerns for implantable neural stimulators. In this work, the implementation of the charge mode stimulator (ChMS) which aims to store charges in a large capacitor bank and inject charges from bank to tissue is presented. This is an alternative method in the field of electrical stimulation that includes both advantages of the efficiency of conventional voltage mode stimulators (VMS) and the controllability of current mode stimulators (CMS). In addition,

charge balancing is an important issue for the stimulators used in chronic electrical stimulation applications due to electrode dissolution. The proposed structure can balance the injected charge without adding extra off-chip components by utilizing only one capacitor which is saved as a benefit of the inherent integration of charge. The proposed stimulator circuit is implemented by discrete components and the effectiveness of the stimulator system is verified through animal experiments.

PA06

Super-Surce-Follower Low-Pass Filter in 90-nm CMOS Process

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In this thesis, an analog baseband circuit, a low-pass filter (LPF), are presented for wideband mobile communication. The LPF consists of two biquadratic cells in cascade, where the biquadratic cell is based on the super-source-follower architecture.

PA07

A Instrumentation Amplifier Design Based on Cross-Coupled Technique for Urea Biosensor

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In this work, we design a high common-mode rejection ratio (CMRR) and low unity gain frequency (UGF) cross-coupled instrumentation amplifier (CCIA). This design was implemented by the TSMC 0.18μm CMOS process technology. By using the three proposed cross-coupled operational amplifier, the cross-coupled instrumentation amplifier (CCIA) was designed with the power supply to +1.8V and -1.8V. The instrumentation amplifier achieved a voltage gain of 54.54dB with a CMRR of 123dB. This instrumentation amplifier was applied on an array RuO2 urea biosensor as a readout circuit. Moreover, the sensing characteristics of the urea biosensor were analyzed. The experimental results show that our array RuO2 urea biosensor combined with CCIA has good average sensitivity of 1.280 mV/(mg/dL) and linearity of 0.993. With the proposed instrumentation amplifier, an effective measurement system can be achieved due to simplicity, convenience, and low cost.

PA08

Envelope-Tracking Hybrid Power Supply Modulator for Power Amplifier

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A switch-liner-hybrid envelope-tracking (ET) power supply modulator is designed and implemented using TSMC 90-nm CMOS technology for power amplifiers (PAs) in modern wireless communications with high peak-to-average-power-ratio. The supply modulator consists of a wideband linear amplifier, a control circuit and a buck converter. Consuming the power of 1.9 mW from the 1.2-V supply, the circuit delivers the output ripple of 41.6 mVpp at the bandwidth of 1 GHz.

PA09

A 37.3 ppm/ºC All-MOS On-Chip Relaxation Oscillator

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This article presents a novel design of RC-less (Resistor and Capacitor-less) relaxation oscillator circuit that has achieved 37.3 ppm/ºC of temperature coefficient. In this design, the main current biasing circuit for the oscillator is designed to be CTAT (complementary to absolute temperature) through a long channel MOSFET to compensate for the inherent PTAT (proportional to absolute temperature) of oscillator circuit. It has achieved an average frequency of 2.98 MHz at 89.6 µW power consumptions in an active area of 0.510 mm2 over a temperature range of 0 to 100ºC.

PA10

Minimum-Phase FIR Feedback in Discrete-Time Hybrid Sturdy MASH-21 Delta-Sigma Modulator for Audio Application

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This paper presents a discrete-time hybrid sturdy MASH-21(HSMASH-21) single-bit delta-sigma (ΔΣ) modulator for audio applications. The modulator uses inverting and noninverting switched-capacitor integrators to eliminate first-stage quantization noise in 0.18um CMOS technology. The simulation

results show that the proposed modulator achieves 96.83 dB Signal to Noise and Distortion Ratio (SNDR) in 24 kHz signal bandwidth with a sampling frequency of 6.144 MHz and costs 1.38 mW at a supply voltage of 1.8 V.

PA11

A 10-bit 160-kS/s Hybrid SAR-VCO ADC for Multi-channel Neural Recording System

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This paper presents a hybrid analog-to-digital converter (ADC) combining successive approximation registers (SAR) with a voltage-controlled ring oscillator (VCO) for the multi-channel neural recording. The proposed coarse-fine architecture can not only save the capacitor area but also reduce the input capacitor load of the multi-channel analog front-end (AFE), which is beneficial for low power design in a system overview. For a larger VCO tuning gain (KVCO), a ring oscillator with the feedforward cross-coupling structure has been used to further reduce the power consumption in the VCO-based fine ADC. Simulation results show that the proposed hybrid SAR-VCO ADC operating at 160-kS/s can achieve a signal-to-noise and distortion ratio (SNDR) of 56.82 dB while consuming 14.92 μW under 1.2/1 V supply, where the capacitor array is much less than a pure 10-bit SAR ADC and hence relax the requirement of driving ability to the multi-channel AFEs.

PA12

12-Bit 5-MS/s Successive Approximation Register ADC with Digital Error Correction and Non-Binary Multiple-LSB-Redundant Capacitors

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This paper presents a 12-bit 5-MS/s successive approximation register (SAR) analog-to-digital converter (ADC) with digital error correction and non-binary multiple-LSB-redundant capacitor, which is fabricated in TSMC 0.18-μm 1P6M CMOS process. The differential input performs with low input noise to have good ability compared to traditional single-ended input. Besides, the switching procedure maintains the common-mode voltage of the comparator with two-terminal capacitor switching and achieves the function of recovery correction with multiple capacitor arrays. In view of the recovery correction function of the capacitor array, two separate capacitors are considered not only to reduce the number of unit capacitors and the chip area, but also to reduce the mismatched errors by using the non-binary multiple elements. The pre-simulated results show that the SFDR, SNDR, ENOB, power consumption, and chip area are 75.82 dB, 71.68 dB, 11.61 bits, 6.25 mW, and 0.589 mm2, respectively, at a supply voltage of 3.3 V, input frequency of 200 kHz, and sampling rate of 5 MS/s.

PA13

A 12bits ENOB 312.5kHz Bandwidth Oversampling SAR ADC with Zero Static Power for CMOS Image Sensor Application

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In this paper, a zero static power oversampling successive approximation register (SAR) analog-to-digital converter (ADC) is proposed for CMOS image sensor application. For precise conversion of optical signal with low power consumption, the proposed SAR ADC employ Passive Noise Shaping structure combining with Data Weighted Averaging (DWA) and Mismatch Error Shaping (MES) techniques. With passive noise shaping structure, the oversampling SAR ADC does not need operational amplifier (OPAMP) for integrator, thus consuming low power. Meanwhile, a zero static current flash ADC is proposed to be the coarse ADC in the two-stage flash-SAR structure. The oversampling SAR ADC operates at 10MS/s, consumes 281.3uW and achieves 12-ENOB in 312.5kHz bandwidth in post-simulation under TSMC 90-nm fabrication.

PA14

A Multi-bit Calibration Algorithm for SAR ADC Chip

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A faster multi-bit calibration algorithm for Successive Approximation Register Analog-to-Digital Converter (SAR ADC) has been proposed in this research work. In the capacitor array of the SAR ADC architecture, the output resolution is inaccurate due to the mismatch of capacitance values. Therefore, a multi-bit calibration algorithm is proposed here. It performs to calculate matrix data in the iterative method, and obtains the mismatched error value. Finally, it compensates for the mismatch error value and corrects it through the digital code to accurate the mismatch capacitance of the circuit. To verify this method, the designed SAR ADC chip is implemented using TSMC's 0.18-μm 1P6M process. Whereas the supply voltage is 3.3V, the chip area is 1.435mm^2 and the core circuit area is 0.429μm^2, the effective number of bits is 8.96-bit, and the power consumption is 4.199μW. At the sampling frequency is 2.048 kHz, the input frequency is 11 Hz, the post-simulation data calibration results show that the multi-bit calibration algorithm can correct the signal-to-noise distortion ratio from 49.97 dB back to 54.83 dB, the effective number of bits from 8.02-bit back to 8.82-bit. It can be integrated into digital circuits in the future.

PA15

A Hysteresis-Current-Hybrid-Controlled Buck Converter using New-Type DCR Currnet-Sensing Techniques

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This paper proposed an improved-hysteresis-current-controlled buck converter with new type DCR current-sensing techniques. This control circuit used a hysteresis-current control circuit to achieve fast transient response and a new type of DCR current sensing circuit which reduced the power consumption and increased the overall system efficiency. This converter was fabricated with TSMC 0.18μm 1P6M process. The chip area is 1.0247mm×0.858mm. The post-simulation results show the transient response are 1.71μs and 1.16μs during the load current changes from 100mA to 600mA and 600mA to 100mA, respectively. The maximum peak efficiency is 91.7% when the output voltage is 2V and the load current is 300mA.

PA16

Non-Inverting Buck-Boost DC-DC Converter with Mixed-Ripple Adaptive On-Time Control

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A non-inverting buck-boost dc-dc converter with mixed-ripple adaptive on-time control is proposed. With the proposed mode selector, smooth transition between buck mode and boost mode can be achieved. Besides, it makes the efficiency reaches its maximum when the input voltage approaches the output voltage. The proposed chip was implemented by using a 0.35 μm CMOS 2P4M 3.3V/5V mixed-signal polycide process. The input voltage may range from 2.5 to 5.0 V, and the output voltage is regulated at 3.3V. According to the measured results, the maximal conversion efficiency is 97.8%

PA17

Design of A Hysteretic-Controlled Buck Converter with New Integral Current-Sensing Techniques

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This paper presents a hysteretic-controlled buck converter with new integral current-sensing. The proposed converter achieves fast transient response and a wide output voltage range. The proposed buck converter is fabricated with TSMC 0.18μm 1P6M CMOS technology, and the chip area is 1.107 mm x 0.851 mm. The measured results show that the output voltage is 1.8V, the load current changes from 50mA to 500mA, and the transient response from 50mA to 500mA is 2 μs and 2.4 μs, respectively. When the load current is 300mA, the maximum power efficiency is 93.65%.

PA18

An Adaptive On-Time Controlled Buck Converter with New-DCR-Current-Sensing Techniques

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This paper presents an adaptive on-time controlled buck converter with new-DCR-current-sensing techniques. The proposed converter achieves high efficiency and fast transient response. The proposed converter is fabricated with TSMC 0.18μm 1P6M process, and the chip area is 1.057 mm×0.773 mm. The output load current range is 50~600mA. The load transient response times are about 2.6 μs and 2.1 μs when the load currents are light to heavy and heavy to light, respectively. The maximum peak efficiency is 90.20% when the output voltage is 2.5V and the load current is 300mA.

PA19

Radio Frequency Energy Harvesting Chip for ISM-915 Wireless Transmitter

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This paper presents a radio frequency (RF) energy harvesting chip for ISM-915 wireless transmitter, which includes the matching network, rectifier, over-voltage protection circuit and low-power low-dropout (LDO) voltage regulator. In the input matching circuit, the maximum power transfer and maximum conversion efficiency are completed with those matched components, which are manufactured by muRata company. In the rectifier circuit, a modified differential rectifier circuit is used to convert the RF signal into DC voltage with boosting function. Besides, the native MOS is used to implement the multiplier rectifier with low threshold voltage. An over-voltage protection circuit is considered to prevent the high-voltage damage from the front-end RF circuit. Finally, a low-power LDO is used to produce a stable output voltage, which is used to charge the load. The proposed RF harvesting chip is fabricated in TSMC 0.18-μm 1P6M CMOS process. According to the simulated results, the rectifier conversion efficiency is about 36.5% and the maximum system conversion efficiency is approximately 27%, which were achieved with respect to input powers of 3 dBm and -1 dBm, respectively, at the radio frequency of 915 MHz. The low-power low-dropout linear regulator stabilizes the output voltage at 1.47 V and the power consumption varies from 36.5 μW to 47.5 μW. The output power and chip area are 217.5 μW and 0.832×0.408 mm2, respectively.

PA20

A current-mode buck converter with V-cubic-controlled Techniques

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A current-mode buck converter with V-cubic-controlled technique is proposed. The proposed architecture can accelerate its transient response and reduce the magnitude of the output ripple. The current Isen is sensed through the current sensing circuit, and the voltage VF is generated through the resistor RF. The HVC circuit can detect the overshoot voltage and undershoot voltage of VF, and make the system transition by detecting the change of the voltage, so that the power transistor can be turned on in advance. The AOT control can fix the conduction time of the circuit and play a very important part in the circuit. The transient response can be effectively improved by some ripple-based control methods. For example, constant on-time control, adaptive on-time control, and hysteretic, which can directly affect the output waveform without compensation, allowing the circuit to achieve a fast response time.[2]-[4] The proposed buck converter has been used in TSMC 0.18μm 1P6M CMOS processes with the area of 1.1mm^2 . The post-simulation results show the transient time are both under 2 μs when the load current changes between 50mA and 500mA. The peak efficiency is 92.8% while the load current is 400mA.

PA21

A wide-range and high-speed Phase-Locked Loop based on Altera FPGA Analysis and Implement

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As the process evolves, the functions of integrated circuits become more complex and develop toward higher frequencies. To cope with such a situation, how to provide the chip with an internal clock signal with higher frequency, low jitter, and can resist the influence of noise and influence of Precess, Voltage, and Temperature (PVT) has become an increasingly important research topic. This paper proposes an All-Digital Phase-Locked Loop (ADPLL) based on the internal structure of the Field Programmable Gate Array (FPGA). Using the Looked-up Table structure and the hardware description language (HDL) Verilog to build a high-frequency digitally controlled oscillator (DCO), and design a frequency divider that can freely adjust the locking multiple. In the pre-sim results, it can be seen that the ADPLL locks to 270MHz at a multiplier of 6.

PA22

18-GHz Subsampling Phase-Locked Loop for Quantum Computing

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A 18 GHz sub-sampling PLL is designed and implemented using TSMC 90-nm CMOS technology for the application of semiconductor spin-qubit quantum computers. As the key building block of the controller in the quantum computer, this signal source needs to achieve the frequency noise of 35 〖kHz〗 _rms and therefore the sub-sampling PLL architecture is adopted. The sub-sampling PLL delivers the 18 GHz signal with the in-band phase noise of -116 dBc/Hz at 300 °K by consuming the power of 15.22 mW and the chip area of 1.01 〖mm〗 ^2. The locking time is 1.5 μs.

PA23

6-GHz Sub-Sampling Phase-Locked Loop for Quantum Computing

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A 6 GHz sub-sampling phase-locked loop to control the microwave signals for quantum computers. The SSPLL is implemented using TSMC 90-nm CMOS technology. The NMOS VCO covers the frequency range from 5.95 GHz to 6.05 GHz. The VCO achieves the phase noise of -124.7 dBc/Hz at 1 MHz frequency offset and -144.8 dBc/Hz at 10 MHz frequency offset. Consuming the power of 20 mW and the chip area of 1.97 mm^2. The SSPLL delivers the 6 GHz signal and exhibits the in-band phase noise of -122 dBc/Hz at 100 KHz frequency offset and the out-band phase noise is -135 dBc/Hz at 10 MHz frequency offset.

PA24

Quadrature All-Pass Filter and 8-bit IDAC for 31-33GHz Vector-Sum Phase Shifter

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A 31-33 GHz vector sum phase shifter topology integrated with digital control, using a quadrature all pass filter (QAF) along with an analog differential adder and 8-bit IDAC, provides the continuous phase shift of 360°. As an active circuit, the vector adder is designed to compensate the losses of passive elements while the impedance matching between the QAF and the vector adder is optimized. 8-bit IDAC plays the rule of gain controls of the I path and Q path in adder, for improving the accuracy of the phase shifter, the influence of the process, voltage and temperature variations on the IDAC should be considered.

PA25

24 GHz Quadrature VCO Integrated with Woven Structure Capacitors in 40-nm CMOS

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This paper presents a quadrature LC voltagecontrolled oscillator (LC-QVCO) design which utilizes defected ground under path to improve the phase noise and output power. The proposed quadrature VCO mainly uses two NMOS crosscoupled oscillators operating at 24 GHz. Two coupling transistors which operate in parallel to the VCO core transistors are used for injecting output phase to divide the output to quadrature. Performance analysis of the proposed oscillators shows that the defected ground method not only improves Q factor of coupling transistors, but also increase VCO output voltage swing. With The varactor set is switchable by using a transmission gate such that the tuning range can be extended. The proposed VCO is designed, implemented, and fully evaluated on the wafer in 40-nm CMOS technology. The center frequency of proposed VCO is 24 GHz with the tuning range of 14.77 %. This VCO provides the highest frequency of 26.32 GHz and the corresponding output power of -6.15 dBm. The VCO consumes 29.9 mW from a 0.9-V supply and exhibits the phase noise of -86.14 dBc/Hz and FOM of -165 at 1 MHz offset.

PA26

The 28-30 GHz RF front-end for Millimeter Wave Absorption Based Non-Invasive Glucose System

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A 28-30 GHz CMOS RF front-end is designed and implemented using 90-nm CMOS technology for non-invasive glucose sensing system. The LNA is delivered the power gain of 24 dB. The mixer provides frequency translation to down convert the signal from 28-30 GHz to 10 MHz with conversion gain of 7.8 dB. The RF front-end achieves the gain of 25.43 dB and P1dB of -32.97 dBm at 29 GHz, and consuming the power of 38.18 mW.

PA27

Design of 1 GHz Ultra-Low Power Phase Lock Loop in 0.18 μm CMOS Technology

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This paper presents the design of an ultra-low power phase lock loop(PLL) at 1 V supply using the TSMC 0.18 μm CMOS process. By modifying the delay cell and true single-phase-clock(TSPC) logic circuit, the proposed PLL can work precisely with low-jitter six-phase outputs at 1 GHz high speed under low voltage. First, a cross-coupled delay cell without tail current is used for a three-stage ring Voltage-Controlled Oscillator (VCO). A delay cell without tail current can maximize the output swing of VCO and generate rail-to-rail output signal. Second, to lower the clock jitter generated by the VCO under low voltage, the delay cell is designed with a low KVCO. Finally, this work adopts dynamic TSPC logic instead of current mode logic (CML) to reduce power consumption and provides the operation of divide-by-32 in the feedback path. The proposed PLL achieves an ultra-low total power of 0.446 mW at a 1 V supply with 0.8 μs locking time at a 31.25 MHz reference clock. With a three-stage ring VCO, the PLL can provide 2.31 ps low-RMS-jitter rail-to-rail six-phase outputs at 1 GHz.