Poster Session

Analog & RF

PA01

A CMOS Algae Growth Period to Duty Cycle Converter for Monitoring Algae Growth Status Applications

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A CMOS algae growth period converter is newly used for applications of monitoring algae growth status. The proposed converter can transform algae growth period into duty cycle linearly. Through the duty cycle of this converter, the algae growth status could be easily and quickly obtained. A wide rail-to-rail voltage to current converter and the adjustment sensitivity circuits are designed to be adaptively used in different kinds of algae growth environment. The wide-range differential voltage is -1.5 to 1.5 V, the corresponding range of output duty cycle was 1.46 to 98.4643 %. The various sensitivities of the proposed converter were 23.496, 27.378, 32.804, and 41.209%/V. The proposed chip could be used for monitoring algae growth status applications.

PA02

A Temperature Compensation Method for Potentiometric Biosensors Based on Arrayed RuO2 Ascorbic Acid Sensing Thin Film

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The temperature effect is analyzed for the ascorbic acid (AA) biosensor based on enzymatic ascorbate oxidase (AO). To reduce this non-ideal effect, a novel temperature compensation circuit was implemented by TSMC 180nm CMOS process. By applying the proposed circuit, the temperature coefficients (TCs) with five concentrations of AA were suppressed below 201 μV/°C. The TC of the normal level of AA (0.0312 mM) in the human body was 188 μV/°C, in the temperature range from 25°C to 55°C. At present, the experiments were still in the stage of in vitro measurement.

PA03

A CMOS with Auto-High Background Immunity Position-Sensitive Detector (PSD) for High Background Light Environment

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In this paper, a CMOS with auto-high background immunity position-sensitive detector (PSD) is newly used for high background light environment. The proposed approach can successfully solve the impact of high background light on PSD. As proven by simulations, if the problem of high background light on PSD in real environment is not solved, the maximum linear error of the PSD will be over 45.25% when the intensity of background light becomes higher than 5 nA. After performing the proposed auto-high background immunity circuits, the maximum linear error can be reduced to below 1% while the intensity of background light is 40 nA. The proposed PSD could be used for high background light environment.

PA04

A Low-Temperature Variation Reference Current Source with Digital Counting Auto-Calibration Scheme

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This paper designs a reference current source that can automatically correct without being affected by temperature. It could be applied to an operational amplifier in analog-to-digital converters (ADC) to provide a stable bias condition. With a supply voltage-independent current reference, the reference current is employed in the current-controlled oscillator (CCO) to generate a clock signal depending on the current. Further, the clock compares with the reference signal provided by the quartz crystal oscillator for frequency detecting. The binary search algorithm determines the reference current by oscillating frequency change caused by the environmental deviation. The design environment of this circuit operates under the conditions of 1.8V supply voltage and -100°C to +200°C of the temperature range in using the UMC 0.18um CMOS process. Thus, it would achieve a self-healing reference current source with the low-temperature variation used in space environments.

PA05

A Charge-mode Neural Stimulator with Active Charge Balancing for Electrical Stimulation Applications

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Energy efficiency and the problem of safety are two major concerns for implantable neural stimulators. In this work, the implementation of the charge mode stimulator (ChMS) which aims to store charges in a large capacitor bank and inject charges from bank to tissue is presented. This is an alternative method in the field of electrical stimulation that includes both advantages of the efficiency of conventional voltage mode stimulators (VMS) and the controllability of current mode stimulators (CMS). In addition,

charge balancing is an important issue for the stimulators used in chronic electrical stimulation applications due to electrode dissolution. The proposed structure can balance the injected charge without adding extra off-chip components by utilizing only one capacitor which is saved as a benefit of the inherent integration of charge. The proposed stimulator circuit is implemented by discrete components and the effectiveness of the stimulator system is verified through animal experiments.

PA06

Super-Surce-Follower Low-Pass Filter in 90-nm CMOS Process

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In this thesis, an analog baseband circuit, a low-pass filter (LPF), are presented for wideband mobile communication. The LPF consists of two biquadratic cells in cascade, where the biquadratic cell is based on the super-source-follower architecture.

PA07

A Instrumentation Amplifier Design Based on Cross-Coupled Technique for Urea Biosensor

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In this work, we design a high common-mode rejection ratio (CMRR) and low unity gain frequency (UGF) cross-coupled instrumentation amplifier (CCIA). This design was implemented by the TSMC 0.18μm CMOS process technology. By using the three proposed cross-coupled operational amplifier, the cross-coupled instrumentation amplifier (CCIA) was designed with the power supply to +1.8V and -1.8V. The instrumentation amplifier achieved a voltage gain of 54.54dB with a CMRR of 123dB. This instrumentation amplifier was applied on an array RuO2 urea biosensor as a readout circuit. Moreover, the sensing characteristics of the urea biosensor were analyzed. The experimental results show that our array RuO2 urea biosensor combined with CCIA has good average sensitivity of 1.280 mV/(mg/dL) and linearity of 0.993. With the proposed instrumentation amplifier, an effective measurement system can be achieved due to simplicity, convenience, and low cost.

PA08

Envelope-Tracking Hybrid Power Supply Modulator for Power Amplifier

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A switch-liner-hybrid envelope-tracking (ET) power supply modulator is designed and implemented using TSMC 90-nm CMOS technology for power amplifiers (PAs) in modern wireless communications with high peak-to-average-power-ratio. The supply modulator consists of a wideband linear amplifier, a control circuit and a buck converter. Consuming the power of 1.9 mW from the 1.2-V supply, the circuit delivers the output ripple of 41.6 mVpp at the bandwidth of 1 GHz.

PA09

A 37.3 ppm/ºC All-MOS On-Chip Relaxation Oscillator

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This article presents a novel design of RC-less (Resistor and Capacitor-less) relaxation oscillator circuit that has achieved 37.3 ppm/ºC of temperature coefficient. In this design, the main current biasing circuit for the oscillator is designed to be CTAT (complementary to absolute temperature) through a long channel MOSFET to compensate for the inherent PTAT (proportional to absolute temperature) of oscillator circuit. It has achieved an average frequency of 2.98 MHz at 89.6 µW power consumptions in an active area of 0.510 mm2 over a temperature range of 0 to 100ºC.

PA10

Minimum-Phase FIR Feedback in Discrete-Time Hybrid Sturdy MASH-21 Delta-Sigma Modulator for Audio Application

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This paper presents a discrete-time hybrid sturdy MASH-21(HSMASH-21) single-bit delta-sigma (ΔΣ) modulator for audio applications. The modulator uses inverting and noninverting switched-capacitor integrators to eliminate first-stage quantization noise in 0.18um CMOS technology. The simulation

results show that the proposed modulator achieves 96.83 dB Signal to Noise and Distortion Ratio (SNDR) in 24 kHz signal bandwidth with a sampling frequency of 6.144 MHz and costs 1.38 mW at a supply voltage of 1.8 V.

PA11

A 10-bit 160-kS/s Hybrid SAR-VCO ADC for Multi-channel Neural Recording System

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This paper presents a hybrid analog-to-digital converter (ADC) combining successive approximation registers (SAR) with a voltage-controlled ring oscillator (VCO) for the multi-channel neural recording. The proposed coarse-fine architecture can not only save the capacitor area but also reduce the input capacitor load of the multi-channel analog front-end (AFE), which is beneficial for low power design in a system overview. For a larger VCO tuning gain (KVCO), a ring oscillator with the feedforward cross-coupling structure has been used to further reduce the power consumption in the VCO-based fine ADC. Simulation results show that the proposed hybrid SAR-VCO ADC operating at 160-kS/s can achieve a signal-to-noise and distortion ratio (SNDR) of 56.82 dB while consuming 14.92 μW under 1.2/1 V supply, where the capacitor array is much less than a pure 10-bit SAR ADC and hence relax the requirement of driving ability to the multi-channel AFEs.

PA12

12-Bit 5-MS/s Successive Approximation Register ADC with Digital Error Correction and Non-Binary Multiple-LSB-Redundant Capacitors

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This paper presents a 12-bit 5-MS/s successive approximation register (SAR) analog-to-digital converter (ADC) with digital error correction and non-binary multiple-LSB-redundant capacitor, which is fabricated in TSMC 0.18-μm 1P6M CMOS process. The differential input performs with low input noise to have good ability compared to traditional single-ended input. Besides, the switching procedure maintains the common-mode voltage of the comparator with two-terminal capacitor switching and achieves the function of recovery correction with multiple capacitor arrays. In view of the recovery correction function of the capacitor array, two separate capacitors are considered not only to reduce the number of unit capacitors and the chip area, but also to reduce the mismatched errors by using the non-binary multiple elements. The pre-simulated results show that the SFDR, SNDR, ENOB, power consumption, and chip area are 75.82 dB, 71.68 dB, 11.61 bits, 6.25 mW, and 0.589 mm2, respectively, at a supply voltage of 3.3 V, input frequency of 200 kHz, and sampling rate of 5 MS/s.

PA13

A 12bits ENOB 312.5kHz Bandwidth Oversampling SAR ADC with Zero Static Power for CMOS Image Sensor Application

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In this paper, a zero static power oversampling successive approximation register (SAR) analog-to-digital converter (ADC) is proposed for CMOS image sensor application. For precise conversion of optical signal with low power consumption, the proposed SAR ADC employ Passive Noise Shaping structure combining with Data Weighted Averaging (DWA) and Mismatch Error Shaping (MES) techniques. With passive noise shaping structure, the oversampling SAR ADC does not need operational amplifier (OPAMP) for integrator, thus consuming low power. Meanwhile, a zero static current flash ADC is proposed to be the coarse ADC in the two-stage flash-SAR structure. The oversampling SAR ADC operates at 10MS/s, consumes 281.3uW and achieves 12-ENOB in 312.5kHz bandwidth in post-simulation under TSMC 90-nm fabrication.

PA14

A Multi-bit Calibration Algorithm for SAR ADC Chip

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A faster multi-bit calibration algorithm for Successive Approximation Register Analog-to-Digital Converter (SAR ADC) has been proposed in this research work. In the capacitor array of the SAR ADC architecture, the output resolution is inaccurate due to the mismatch of capacitance values. Therefore, a multi-bit calibration algorithm is proposed here. It performs to calculate matrix data in the iterative method, and obtains the mismatched error value. Finally, it compensates for the mismatch error value and corrects it through the digital code to accurate the mismatch capacitance of the circuit. To verify this method, the designed SAR ADC chip is implemented using TSMC's 0.18-μm 1P6M process. Whereas the supply voltage is 3.3V, the chip area is 1.435mm^2 and the core circuit area is 0.429μm^2, the effective number of bits is 8.96-bit, and the power consumption is 4.199μW. At the sampling frequency is 2.048 kHz, the input frequency is 11 Hz, the post-simulation data calibration results show that the multi-bit calibration algorithm can correct the signal-to-noise distortion ratio from 49.97 dB back to 54.83 dB, the effective number of bits from 8.02-bit back to 8.82-bit. It can be integrated into digital circuits in the future.

PA15

A Hysteresis-Current-Hybrid-Controlled Buck Converter using New-Type DCR Currnet-Sensing Techniques

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This paper proposed an improved-hysteresis-current-controlled buck converter with new type DCR current-sensing techniques. This control circuit used a hysteresis-current control circuit to achieve fast transient response and a new type of DCR current sensing circuit which reduced the power consumption and increased the overall system efficiency. This converter was fabricated with TSMC 0.18μm 1P6M process. The chip area is 1.0247mm×0.858mm. The post-simulation results show the transient response are 1.71μs and 1.16μs during the load current changes from 100mA to 600mA and 600mA to 100mA, respectively. The maximum peak efficiency is 91.7% when the output voltage is 2V and the load current is 300mA.

PA16

Non-Inverting Buck-Boost DC-DC Converter with Mixed-Ripple Adaptive On-Time Control

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A non-inverting buck-boost dc-dc converter with mixed-ripple adaptive on-time control is proposed. With the proposed mode selector, smooth transition between buck mode and boost mode can be achieved. Besides, it makes the efficiency reaches its maximum when the input voltage approaches the output voltage. The proposed chip was implemented by using a 0.35 μm CMOS 2P4M 3.3V/5V mixed-signal polycide process. The input voltage may range from 2.5 to 5.0 V, and the output voltage is regulated at 3.3V. According to the measured results, the maximal conversion efficiency is 97.8%

PA17

Design of A Hysteretic-Controlled Buck Converter with New Integral Current-Sensing Techniques

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This paper presents a hysteretic-controlled buck converter with new integral current-sensing. The proposed converter achieves fast transient response and a wide output voltage range. The proposed buck converter is fabricated with TSMC 0.18μm 1P6M CMOS technology, and the chip area is 1.107 mm x 0.851 mm. The measured results show that the output voltage is 1.8V, the load current changes from 50mA to 500mA, and the transient response from 50mA to 500mA is 2 μs and 2.4 μs, respectively. When the load current is 300mA, the maximum power efficiency is 93.65%.

PA18

An Adaptive On-Time Controlled Buck Converter with New-DCR-Current-Sensing Techniques

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This paper presents an adaptive on-time controlled buck converter with new-DCR-current-sensing techniques. The proposed converter achieves high efficiency and fast transient response. The proposed converter is fabricated with TSMC 0.18μm 1P6M process, and the chip area is 1.057 mm×0.773 mm. The output load current range is 50~600mA. The load transient response times are about 2.6 μs and 2.1 μs when the load currents are light to heavy and heavy to light, respectively. The maximum peak efficiency is 90.20% when the output voltage is 2.5V and the load current is 300mA.

PA19

Radio Frequency Energy Harvesting Chip for ISM-915 Wireless Transmitter

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This paper presents a radio frequency (RF) energy harvesting chip for ISM-915 wireless transmitter, which includes the matching network, rectifier, over-voltage protection circuit and low-power low-dropout (LDO) voltage regulator. In the input matching circuit, the maximum power transfer and maximum conversion efficiency are completed with those matched components, which are manufactured by muRata company. In the rectifier circuit, a modified differential rectifier circuit is used to convert the RF signal into DC voltage with boosting function. Besides, the native MOS is used to implement the multiplier rectifier with low threshold voltage. An over-voltage protection circuit is considered to prevent the high-voltage damage from the front-end RF circuit. Finally, a low-power LDO is used to produce a stable output voltage, which is used to charge the load. The proposed RF harvesting chip is fabricated in TSMC 0.18-μm 1P6M CMOS process. According to the simulated results, the rectifier conversion efficiency is about 36.5% and the maximum system conversion efficiency is approximately 27%, which were achieved with respect to input powers of 3 dBm and -1 dBm, respectively, at the radio frequency of 915 MHz. The low-power low-dropout linear regulator stabilizes the output voltage at 1.47 V and the power consumption varies from 36.5 μW to 47.5 μW. The output power and chip area are 217.5 μW and 0.832×0.408 mm2, respectively.

PA20

A current-mode buck converter with V-cubic-controlled Techniques

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A current-mode buck converter with V-cubic-controlled technique is proposed. The proposed architecture can accelerate its transient response and reduce the magnitude of the output ripple. The current Isen is sensed through the current sensing circuit, and the voltage VF is generated through the resistor RF. The HVC circuit can detect the overshoot voltage and undershoot voltage of VF, and make the system transition by detecting the change of the voltage, so that the power transistor can be turned on in advance. The AOT control can fix the conduction time of the circuit and play a very important part in the circuit. The transient response can be effectively improved by some ripple-based control methods. For example, constant on-time control, adaptive on-time control, and hysteretic, which can directly affect the output waveform without compensation, allowing the circuit to achieve a fast response time.[2]-[4] The proposed buck converter has been used in TSMC 0.18μm 1P6M CMOS processes with the area of 1.1mm^2 . The post-simulation results show the transient time are both under 2 μs when the load current changes between 50mA and 500mA. The peak efficiency is 92.8% while the load current is 400mA.

PA21

A wide-range and high-speed Phase-Locked Loop based on Altera FPGA Analysis and Implement

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As the process evolves, the functions of integrated circuits become more complex and develop toward higher frequencies. To cope with such a situation, how to provide the chip with an internal clock signal with higher frequency, low jitter, and can resist the influence of noise and influence of Precess, Voltage, and Temperature (PVT) has become an increasingly important research topic. This paper proposes an All-Digital Phase-Locked Loop (ADPLL) based on the internal structure of the Field Programmable Gate Array (FPGA). Using the Looked-up Table structure and the hardware description language (HDL) Verilog to build a high-frequency digitally controlled oscillator (DCO), and design a frequency divider that can freely adjust the locking multiple. In the pre-sim results, it can be seen that the ADPLL locks to 270MHz at a multiplier of 6.

PA22

18-GHz Subsampling Phase-Locked Loop for Quantum Computing

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A 18 GHz sub-sampling PLL is designed and implemented using TSMC 90-nm CMOS technology for the application of semiconductor spin-qubit quantum computers. As the key building block of the controller in the quantum computer, this signal source needs to achieve the frequency noise of 35 〖kHz〗 _rms and therefore the sub-sampling PLL architecture is adopted. The sub-sampling PLL delivers the 18 GHz signal with the in-band phase noise of -116 dBc/Hz at 300 °K by consuming the power of 15.22 mW and the chip area of 1.01 〖mm〗 ^2. The locking time is 1.5 μs.

PA23

6-GHz Sub-Sampling Phase-Locked Loop for Quantum Computing

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A 6 GHz sub-sampling phase-locked loop to control the microwave signals for quantum computers. The SSPLL is implemented using TSMC 90-nm CMOS technology. The NMOS VCO covers the frequency range from 5.95 GHz to 6.05 GHz. The VCO achieves the phase noise of -124.7 dBc/Hz at 1 MHz frequency offset and -144.8 dBc/Hz at 10 MHz frequency offset. Consuming the power of 20 mW and the chip area of 1.97 mm^2. The SSPLL delivers the 6 GHz signal and exhibits the in-band phase noise of -122 dBc/Hz at 100 KHz frequency offset and the out-band phase noise is -135 dBc/Hz at 10 MHz frequency offset.

PA24

Quadrature All-Pass Filter and 8-bit IDAC for 31-33GHz Vector-Sum Phase Shifter

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A 31-33 GHz vector sum phase shifter topology integrated with digital control, using a quadrature all pass filter (QAF) along with an analog differential adder and 8-bit IDAC, provides the continuous phase shift of 360°. As an active circuit, the vector adder is designed to compensate the losses of passive elements while the impedance matching between the QAF and the vector adder is optimized. 8-bit IDAC plays the rule of gain controls of the I path and Q path in adder, for improving the accuracy of the phase shifter, the influence of the process, voltage and temperature variations on the IDAC should be considered.

PA25

24 GHz Quadrature VCO Integrated with Woven Structure Capacitors in 40-nm CMOS

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This paper presents a quadrature LC voltagecontrolled oscillator (LC-QVCO) design which utilizes defected ground under path to improve the phase noise and output power. The proposed quadrature VCO mainly uses two NMOS crosscoupled oscillators operating at 24 GHz. Two coupling transistors which operate in parallel to the VCO core transistors are used for injecting output phase to divide the output to quadrature. Performance analysis of the proposed oscillators shows that the defected ground method not only improves Q factor of coupling transistors, but also increase VCO output voltage swing. With The varactor set is switchable by using a transmission gate such that the tuning range can be extended. The proposed VCO is designed, implemented, and fully evaluated on the wafer in 40-nm CMOS technology. The center frequency of proposed VCO is 24 GHz with the tuning range of 14.77 %. This VCO provides the highest frequency of 26.32 GHz and the corresponding output power of -6.15 dBm. The VCO consumes 29.9 mW from a 0.9-V supply and exhibits the phase noise of -86.14 dBc/Hz and FOM of -165 at 1 MHz offset.

PA26

The 28-30 GHz RF front-end for Millimeter Wave Absorption Based Non-Invasive Glucose System

Zhong-Da Wu and Hsiao-Chin Chen
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A 28-30 GHz CMOS RF front-end is designed and implemented using 90-nm CMOS technology for non-invasive glucose sensing system. The LNA is delivered the power gain of 24 dB. The mixer provides frequency translation to down convert the signal from 28-30 GHz to 10 MHz with conversion gain of 7.8 dB. The RF front-end achieves the gain of 25.43 dB and P1dB of -32.97 dBm at 29 GHz, and consuming the power of 38.18 mW.

PA27

Design of 1 GHz Ultra-Low Power Phase Lock Loop in 0.18 μm CMOS Technology

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This paper presents the design of an ultra-low power phase lock loop(PLL) at 1 V supply using the TSMC 0.18 μm CMOS process. By modifying the delay cell and true single-phase-clock(TSPC) logic circuit, the proposed PLL can work precisely with low-jitter six-phase outputs at 1 GHz high speed under low voltage. First, a cross-coupled delay cell without tail current is used for a three-stage ring Voltage-Controlled Oscillator (VCO). A delay cell without tail current can maximize the output swing of VCO and generate rail-to-rail output signal. Second, to lower the clock jitter generated by the VCO under low voltage, the delay cell is designed with a low KVCO. Finally, this work adopts dynamic TSPC logic instead of current mode logic (CML) to reduce power consumption and provides the operation of divide-by-32 in the feedback path. The proposed PLL achieves an ultra-low total power of 0.446 mW at a 1 V supply with 0.8 μs locking time at a 31.25 MHz reference clock. With a three-stage ring VCO, the PLL can provide 2.31 ps low-RMS-jitter rail-to-rail six-phase outputs at 1 GHz.

Digital & System

PD01

Automatic Alignment of Power Traces for Power Analysis

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Data encryption is critical for information security. Previous studies show that power analysis is a powerful tool for side-channel attack against cryptographic modules. Therefore, it is essential to carry out power analysis to assess the vulnerability of cryptographic modules. The success of power analysis relies on aligned power traces, which is not easy without an external trigger point. In this paper, we propose an automatic power trace alignment method so that operations in power traces and be located without external trigger points. Experimental results show that the proposed method can be applied to various ciphers, including AES and RSA.

PD02

Low Complexity and Low Power Sense-Amplifier Flip-Flop for Low Voltage Operation

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A low power and highly reliable sense-amplifier (SA) based flip-flop (FF) with transition completion detection is proposed. The proposed design integrates the generated detection circuit to indicate the completion of SA stage and thus overcoming the operational yield degradation with 2.3% area saving. Simulation results shown that the minimum VDD of our design is 260mV lower than previous design, which means our design can operate even when VDD is in the subthreshold region.

PD03

Edge-Preserving Filter FPGA Design Based on Side-Window Filter

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This paper presents an edge-preserving filter design by using edge detection to reduce the computational complexity of the side window filter. By identifying edge types in advance, the side window filter is unnecessary to produce each result in the same time for comparing. The hardware architecture is implemented on Xilinx's FPGA, which can reduce 86% power consumption, 89% number of LUTs, 67% number of FFs, and 84% number of route nets, respectively. The synthetic results show that this method can reduce the computational complexity of the side window filter and achieve low-cost hardware implementation

PD04

Based on Logarithmic Computing to Design an Embedded CNN Processor

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This paper proposes an embedded CNN processor design that can easily fit into edge devices based on a modified logarithmic computing method using a deficient bit-width representation. For Yolov2, our processing circuit takes only 0.15mm^2 using TSMC 40 nm cell library. The key idea is to apply a low bit-width logarithmic expression to devise a unified, reusable CNN computing kernel that can significantly reduce computing resources. The proposed approach has been extensively evaluated on many famous image classification CNN models (AlexNet, VGG16 and ResNet-18/34) and object detection models (Yolov4). The hardware-implemented results show that our design achieves 20x performance improvement while consuming only minimal computing and storage resources yet attains very high accuracy. The method is thoroughly verified on FPGAs, and the SoC integration is underway with promising results. Our design is excellent for edge computing purposes with extremely efficient resources and energy usage.

PD05

Smart Crop Growth Monitoring based on System Adaptivity and Edge AI

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This work proposes a smart crop growth monitoring system that contains an adaptive cryptography engine to ensure the security of sensor data and an edge artificial intelligence (AI) based estimator to classify the pest and disease severity (PDS) of target crops. Based on the smart system management mechanism, cryptographic functions can be adapted to varying and real-time requirements, while the actuators can be controlled to interact with the physical world to ensure the healthy growth of crops. Experiments show when all the four cryptographic hardware modules, including RTEA32, RTEA64, XTEA32 and XTEA64, are supported, using the adaptive cryptography engine, 72.4% of slice LUTs and 68.4% of slice registers in terms of the Xilinx Zynq-7000 XC7Z020 chip can be saved. Furthermore, using the binarized neural network (BNN) hardware module of the PDS estimator, the recognition accuracy of target crops i.e. dragon fruits can achieve 76.57%. Compared to the microprocessor-based design and the GPU accelerated one, the same BNN architecture on the FPGA can accelerate the frames per second by a factor of 4,919.29 and a factor of 1.08, respectively.

PD06

Hybrid Design of Out-of-order Load/Store Instructions of A Risc-V Superscalar

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In this paper, we present the design of an out-of-order load/store pipeline of the open-source RISC-V superscalar processor, Falco [1]. The original load/store pipeline of Falco only allows in-order execution of memory instructions. However, out-of-order execution of memory instructions is crucial to the performance of superscalars for modern applications. However, the common log-based recovery scheme for speculative mis-prediction usually takes many cycles to recover from a Write-After-Read (WAR) hazard. To improve the load/store pipeline of Falco, we adopt the speculative execution scheme using store sets. In addition, a hybrid recovery mechanism based on the checkpoint snapshots and the log-based instruction rollback is used to reduce the processor recovery time upon mis-prediction. As the experimental results show, the proposed architecture can improve the performance of the original Falco by 18% based on standard benchmarks. The proposed design is verified on a Xilinx FPGA development board and is made open-source for future improvements.

PD07

Low-Complexity Arrhythmia Classification using Phase Portrait of Photoplethysmography with Artificial Neural Network

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To classify the arrhythmias on the wearable devices, the features from phase portrait of photoplethysmography (PPG) with Artificial Neural Network (ANN) are used because of the low computation complexity and high flexibility. By changing the number of the input features in ANN, the suitable number of layers and neurons in the hidden layers for the wearable devices can be found. A set of 17 input features with 3 hidden layers and the set of 8 features with 1 hidden layer can get up to 97.38% and 86.41% accuracies in bradycardia.

PD08

An Energy Efficiency Architecture Design on Sparsity CNN Accelerator

Chung-Bin Wu and Chung-Hsuan Chen
National Chung-Hsing University

Sparse CNN computing has received attention in recent years, especially for mobile devices, or image detection devices that require high image inference per second. This technology can bring faster processing speed and higher energy efficiency. This paper designs an energy-efficient sparse computing architecture, which can average the workload between each Process Engine (PE) when computing sparse images and can reduce the time for PE to grab valid values when the image is extremely sparse. The proposed hardware can achieve 56.43 GOPS and 4.51 Frame/s under the VGG-16 network at 200Mhz, and the Multiply Accumulate Utilization (MACs Utilization) can reach an average of 97.94%.

PD09

Embedded TCP/IP Controller for a RISC-V SoC

Yi-De Lee, Jung-Chun Tsai, and Chun-Jen Tsai
Department of Computer Science, National Yang Ming Chiao Tung University

In this paper, we present the design of an open-source RISC-V application processor with an embedded TCP/IP network module. Traditionally, the TCP/IP stack is a software layer of the OS kernel due to its complex control behavior. However, previous studies show that a hardwired logic can perform TCP/IP control algorithms much more efficiently than a software implementation. However, to allow a processor to invoke a hardware TCP/IP logic efficiently and create compatible API for existing network applications is not a trivial task. This paper proposes an efficient interface logic between the processor core and the hardware TCP/IP stack through user-defined RISC-V instructions. The proposed architecture is implemented and verified on a Xilinx FPGA development board. Experimental results show that the end-to-end packet delay can be reduced by more than 99% using the proposed network module when compared to a software LWIP stack under a FreeRTOS real-time system. Therefore, the proposed architecture can be very useful for deeply-embedded IOT devices where a low-power processor can be used to handle low-latency high throughput IP packet transmissions.

PD10

Edge AI System for Upper Arm Training

Hsiang-Lung Huang and Ya-Hsin Hsueh
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In order to encourage people to exercise in their own homes or private places, this system can help users understand the upper arm training posture correctness of their movements. We build an edge AI motion detection system contains image recognition and a homemade wearable device. In addition to attendant their own action in the real-time on display, users can also see the results of the system's recognition of the movements. When they invention that the correct number of motions has not been accumulated, they can adjust their posture promptly to avoid the incorrect posture for a long time. The combination of image recognition and wearable devices can reduce the misjudgment of movement caused by the environment and other influences. In the era of coronavirus outbreak, this study provides a tool that can help users to check their posture when people choose to exercise at home or in private places without professional guidance.

PD11

Conditional Deep Convolutional GAN for Denoising and Inpainting On-Display Fingerprint

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On-Display Fingerprint (ODF) images are usually quite blurry. Nowadays, ODF smartphone has gradually become a standard configuration in the market, the clarity of the fingerprint image obtained by the ODF sensor will seriously affect the accuracy of fingerprint recognition. Therefore, this paper proposes the Deep Convolutional Generative Adversarial Network (DCGAN) based method to effectively improve the quality of ODF images. Moreover, two self-established ODF Ground Truth (GT) databases are used for training and similarity verification. We finally present three DCGAN series network architectures, namely DCGAN, Conditional DCGAN (CDCGAN), and Reconstruction CDCGAN (RecCDCGAN). In addition, the evaluation is based on the SSIM image similarity score and the NFIQ 2 for fingerprint quality estimation. Experiments show that RecCDCGAN can generate the best clear fingerprint images for blurred ODF images.

PD12

Scalable and Reconfigurable Architecture of Modified KD-Tree ML-Classifier with 5-Point Searching

Xin-Yu Shih and Chen-Yen Song
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This paper proposes a reconfigurable hardware architecture of modified KD-tree machine-learning classifier. As compared to current literature, this hardware is the first KD-tree-like hardware chip implementation. As compared with original KD-tree algorithm, our design can deliver a very low latency in hardware because we do not need the data traversal steps along the binary tree. Meanwhile, this scalable hardware can be easily constructed if supporting a greater number of data instances to be classified. In the chip implementation with TSMC 40-nm CMOS technology, our reconfigurable hardware chip achieves a maximum frequency of 334.5 MHz, only occupying an area of 0.884 mm2 in APR.

PD13

Latency Minimization for MLP Accelerators using an ILP-Based Weight Allocation Method

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It is generally impossible to store all weights into an MLP accelerator because of limited on-chip SRAM capacity. However, the performance can still be improved if a portion of weights are allocated in faster SRAM. In this paper, we first present an analytical method for performance evaluation under different weight allocation approaches. We then propose an ILP-based on-chip weight allocation strategy that can maximize the overall performance. Experiment results show that the proposed strategy constantly outperforms several trivial heuristic methods over a large set of various MLP models, MLP accelerator configurations, and on-chip SRAM capacities.

PD14

A FPGA-based System Integration of DPU Unit and Single Image Fog Removal Method Using Improved Dark Channel Prior

Nguyen Hoang Hai Pham, Zhi-Hao Chen, and Chi-Chia Sun
Department of Electrical Engineering, National Formosa University

The current application of deep learning networks in public monitoring systems and driver assistance systems has made great progress. However, it needs a lot of development effort in order to make these neural networks working effectively in a variety of weather. We propose a system integration solution which includes several accelerated digital image processors and Deep Learning Processing Unit (DPU). These digital image processors employ traditional image processing and single image fog removal based on an improved dark channel prior algorithm to enhance input images, while the DPU can run several pruned and quantized deep learning models. We implemented the system on a Field-Programmable Gate Array (FPGA) platform resulting in high accuracy and low power consumption, which is suitable for edge computing or embedded system applications.

PD15

Energy-efficient and Accurate Object Detection Design on FPGA Platform

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With the innovation of hardware equipment, the development of artificial intelligence has broken through the limitations of the past. Neural networks have been continuously deepening to improve the accuracy of detection, so that the parameters have increased with a proportional rate. In this way, however, high power consumption has followed. Therefore, the design of neural network must consider not only detection accuracy but also energy efficiency. In this paper, we analyzed energy consumption, detection accuracy and execution speed of our neural network model as well as the state-of-the-art models based on an FPGA platform called ZCU-102. We adopt the performance index from Low Power Computer Vision (LPCV) challenge which considers power dissipation, mean Average Precision (mAP) and Frames Per Second (FPS) at the same time to evaluate these models in an overall point of view. Agilev4 can achieve 59.9% of mAP@50 on MS COCO test-dev2017 datasets. If the input frame resolution is turned into 416×416, the processing frame rate can reach 20.7 FPS on ZCU-102. Compared with the state-of-the-art models, the LPCV score of Agilev4-416 is 1475.8 which is 1.56 times of that of YOLOv4-416.

PD16

A 1.46TOPS/W Deep Learning Processor with a Reconfigurable Processing Element array based on SRAM Access Optimization

Liao-Chuan Chen, Zhaofang Li, Yi-Jhen, Lin, and Kea-Tiong Tang
National Tsing Hua University

Deep convolutional neural networks feature numerous parameters, causing data movement to usually dominate the power consumed when computing inferences. This paper proposes an on-chip buffer access optimization method and high-data-reuse architecture that can reduce the power consumed by an on-chip buffer by up to 67.8%. The chip is designed in a TSMC 40 nm process running at 200 MHz and achieves energy efficiency of 1.46 TOPS/W.

PD17

MARSv2: Multicore and Programmable Reconstruction Architecture Using SRAM CIM-Based Accelerator with Lightweight Network

Chia-Yu Hsieh[1], Shih-Ting Lin[1], Yen-Wen Chen[1], Chih-Cheng Lu[2], Meng-Fan Chang[1], and Kea-Tiong Tang[1]
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Computing-in-memory (CIM) systems reduce the degree of large-scale data movement by performing computation on the memory; this avoids a von Neumann bottleneck. Because of its low-power characteristic, CIM has demonstrated great potential for increasing the energy efficiency of edge devices. This paper presents a multicore and programmable reconstruction architecture using static random-access memory (SRAM) CIM-based accelerator with lightweight network. The proposed architecture uses SRAM CIM macro as the processing element, supporting sparse convolutional neural network computing. This architecture achieves 15.16 TOPS/W system energy efficiency and 747.6 GOPS on the CIFAR10 data set.

PD18

Convolution Neural Network Chip Design using Selective Convolution Layer

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Engine(SPE-I) is proposed to efficiently accelerate CNN processing by eliminating most unessential operations based on algorithm-hardware coptimizations. First, we will compare two input image similartity. If similartity is too high, this will be regarded as redundant calculations which will be skipped. The experimental results show that accuracy drops by only 0.12%–1.79%with a 73%–81% multiplicative reduction by compared with original CNN model implementations.

PD19

A Winograd Architecture Design for Edge AI Accelerator

Po-Yao Chung and Wei-Kai Cheng
Department of Information and Computer Engineering, Chung Yuan Christian University

With the development of modern artificial intelligence (AI) technology, convolutional neural networks (CNNs) has been widely used in many application domains. However, as the computation demand of CNNs is dominated by convolution layers, some researches exploit Winograd algorithm to mitigate the number of required multiplications. In this paper, we propose a hardware architecture design based on the Winograd algorithm to reduce the computational complexity of the convolutional layer, and we use an approach different from previous Winograd implementations to optimize the time spent in the Winograd matrix conversion process. Except to the stride one CNN computation, our proposed pipeline architecture can also apply to the stride-2 CNN computation based on a decomposition methodology. Compare the efficiency between executing Winograd algorithm on our proposed architecture and executing sliding window convolution on the Systolic array architecture, experiment results show that our architecture can reduce up to 40% of computation cycles under the same number of multiplier–accumulator (MAC) resource.

PD20

Row Echelon Form Reconfigurable Sparse Matrix Elimination Implementation

Bo-Yi Wu
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With the progress of artificial intelligence (AI), the amount of computation data will continue to rise, and more complex calculations will need to be performed on edge devices. More flexible, reconfigurable processing methods, reduced data storage and computation are increasingly important on edge device systems. This paper implements a hardware architecture to find commonalities between filters in convolutional neural network (CNN). Use reconfigurable hardware to support multiple kernel sizes and utilize a systolic array hardware architecture. The Gaussian-Seidel iterative algorithm finds commonality between filters and recombines the filters using linear combination coefficients. Improved Gaussian-Seidel (GS) iteration algorithm to speed up iteration and hardware usage in systolic array hardware architecture. In order to reduce the size of data storage, use the Linked List Encoding (LNK) method to effectively compress filter data of variable kernel size. The design process is based on Algorithm/Architecture co-design, and the data flow is constructed by analyzing the number of operations, hardware parallelism, memory storage, and data transmission. The experimental results show that enhancing the sparsity on operation arrays can reduce the operation on the Resnet50 model. The sparseness of the matrix means that data storage and computation can be reduced through data compression.

PD21

A Novel Fast-Flying Bird Detection and Identification Based on Configurable AI DPU Processor on FPGA Accelerator Card

Afaroj Ahamad, Chi-Chia Sun, and Hoang Minh Nguyen
Digital System Design Laboratory, National Formosa University

In this article, we proposed a deep learning algorithm for fast-flying bird identification methodology and it is implemented on an embedded platform with an Alveo accelerator card. The Alveo accelerator card provides high bandwidth memory architecture. The novel detection method is divided into two sub-processes, i.e. moving object detection and object identification. Accelerated image processing is used to detect moving objects and configurable neural network inference is used for bird identification. The moving object detection process is based on the principle of frame difference. Afterward, the moving object objects are recorded with their size and position within the image. The confirmed moving object is pushed through a deep learning processor unit (DPU) for classification, resulting in the name of the bird species. The proposed method implemented and tested on Alveo U50 accelerated card can attend high accuracy of up to 81 % with the execution of 289 FPS while processing 960x540 resolution videos, and 84 FPS while processing HD definition (1920x1080) videos, furthermore the DPU execution alone can reach 583 FPS.

PD22

The Multi-Phase Direct Digital Synthesizer Based on Pipelined CORDIC Algorithm for Quantum Computer

Tzu-Hsuan Hsu and Hsiao-Chin Chen
National Taiwan University of Science and Technology

This paper presents a direct digital synthesizer (DDS) for the controller in a quantum computer. In order to reduce the hardware cost, the pipeline coordinate rotation digital computer (CORDIC) is adopted, where the hardware cost can be reduced by 45% and the SFDR > 58 dB is achieved. Moreover, according to the simulation, the multi-phase architecture can be used to boost the output frequency range by at least 14 times.

PD23

Deep Learning Accelerator Integration and Implementation of FPGA Platform Handshake Verification

Chung-Bin Wu and Tzu-wei Chan
National Chung-Hsing University

In today's image CNN accelerators, both the number of network layers and the number of operating parameters are complicated to obtain better recognition results. In order to implement DLA (Deep Learning Accelerator) on the Zynq UltraScale+ MPSoC ZCU102 platform, this paper also proposes a related integrated optimization scheme, which is beneficial to the stability of software and hardware.

PD24

Study of Deep-Learning YOLO-Based Driver Monitor System Design with Embedded GPU Devices

Yen-Sok Poon and Chih-Peng Fan
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To develop a non-contact driver behavior detection system to improve driving safety, in this study, by installing a webcam on the dashboard to detect the driver's behavior, and YOLO-based deep learning technology is used. By using RGB channel images as input, YOLO-based deep learning models such as YOLOv3-tiny, YOLOv3-tiny-3l, YOLO-fastest, and YOLO-fastest-xl are adopted and trained as candidate detectors. Detected behaviors include normal driving, distracted head rotation, drowsiness, eating, and telephone conversations. Experimental results show that YOLO-fastest-xl and its lite version can perform best with multi-category datasets when the same parameters are set. By the embedded software implementation on GPU based devices, the proposed design performs 30 frames per second (FPS) for real-time applications.

PD25

Reconfigurable symmetry pattern in Gabor Filter Using Principal Component Analysis with Microprogrammed Controller

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Abstract-With the increasing popularity of artificial intelligence (AI) as AI requires higher precision and large computation, Different data streams can be generated for different algorithms, which can improve efficiency and flexibility this paper is based on algorithm/architecture Co-design (AAC) [2] using computationally efficient Gabor filters via Principal Component Analysis (PCA). PCA projects filter coefficients onto a more symmetric vector space, then reduces the computation by sharing coefficients. On the other hand, in a trade-off between algorithmic accuracy and computational efficiency, we replaced the first convolutional layer of Resnet50. In our experiments, we observed a slight accuracy drop, which is acceptable.

EDA & Testing

PE01

AN-HRNS: AN-Coded Hierarchical Residue Number System for Neural Network Acceleration and Reliability

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Residue Number Systems (RNS) can simultaneously improve computing acceleration, area reduction and power saving. For reliability-critical applications, disjoint modularization empowers the redundant RNS fault tolerance. However, parallel multiple modular redundancy takes a huge number of converters. In this paper we develop a hierarchical RNS and apply the AN-codes for both sub-RNS error correction and MMR checking. An expanded residue-to-binary converter is developed for highly reduction of the whole multiple-module redundancy decoder. This is the first paper to incorporate AN codes to the RRNS applied in highly-reliable neural networks. From experimental results, only one extra redundant modulus is required. The g=(k+2)(k+1)/2 residue-to-binary converters and g(g-1)/2 comparators can be reduced to only k+1 decoders. From BLER simulations, more than 126 times of MTBF can be achieved.

PE02

Impact of Humidity on ESD Robustness of Integrated Circuits and Systems

Cheng-Yu Liu, Wei-Ching Liao, and Chun-Yu Lin
Department of Electrical Engineering, National Taiwan Normal University

Nowadays the electronic devices may be used everywhere with extreme environment, including very high or low humidity. The effects of humidity on the electrostatic discharge (ESD) robustness of the electronic devices are needed to be studied. In this work, the simple integrated circuits and systems to simulate the electronic devices with various humidity are studied. The impact of the humidity on ESD robustness are found and studied in this paper.

PE03

Efficient Yield Analysis for SRAM-Based System with PDF Consolidation Methodology

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SRAM-based system is one of the most popular design in various applications. However, the high yield request of SRAM system brings difficulties to verification tasks due to high simulation cost for yield estimation. Importance sampling techniques are able to reduce the number of samples in high sigma analysis. However, the complexity is still high if the entire memory system with peripheral circuits are simulated together. To handle this issue, we propose an efficient yield analysis method for the overall SRAM system. Instead of analyzing whole system directly, the proposed methodology evaluating each circuit block first. Then, the interactions of circuit blocks are considered to evaluate the accurate system performance with the prior distribution of each block. In this way, the overall accurate design yield can be obtained easily. The experimental results show that the proposed methodology is able to estimate the design yield of rare failure SRAM designs efficiently with high accuracy.

PE04

Dynamic Power Model for SRAM-Based In-Memory Computing

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Because the demand for low-power equipment is growing up, extending battery life and reducing heat dissipation become important considerations. In recent years, In-Memory Computing (IMC) technology is proposed to solve the bottleneck of data movement in AI edge designs. In order to implement simple computation, the IMC designs often adopt analog operations, which bring new issues to power estimation. Because the complexity of power estimation at transistor-level is often too high for large design, this work proposes a high-level power consumption model to provide different power values for different input patterns. We focus on the effect of switched data bits because it will directly cause current change. Therefore, we propose an efficient approach to record the power consumption with different Hamming distance. As shown in the experimental results, the proposed power model is able to reduce the power estimation time for IMC designs and still retains similar result under different input patterns.

PE05

Aging-aware Computing In-memory Technique for 8T SRAM Multi-bit Dot Product Engine

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Von Neumann architecture which separates the computing logic and the storage area has been considered as the fundamental architecture of nearly all digital computers nowadays. The data intensive applications such as image recognition or cryptography may transfer large amount of data between memory and the computing cores, which causes a well-known von Neumann bottleneck due to the limitation of communication bandwidth. Computing In-Memory (CIM), which directly perform in-situ operations at memory, has been considered as one of the promising solutions to overcome von Neumann bottleneck. Previous researchers have proposed an 8T-SRAM-based CIM architecture to perform multi-bit dot product computations by analog charging/discharging operations. However, such operations are very sensitive to variations as well as aging effects such as Bias Temperature Instability (BTI) and/or Hot Carrier Injection (HCI). To provide a reliable CIM multi-bit dot product engine, in this paper we propose an aging-aware in-memory computing framework which consists of an aging detection method and an aging tolerance technique. Specifically, we apply Dynamic Voltage Frequency Scaling (DVFS) on CIM structure to compensate the current drop due to variations and aging effects. Experimental results show that we can double the lifetime of CIM structure with 1.185x extra power consumption in average.

PE06

2DAN-BNN: Two-Dimensional Error Location for AN-Code Decoders in Binarized Neural Networks

Kuan-Yu Huang, Cheng-Di Tsai, and Tsung-Chu Huang
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AI accelerator, binarized neural network (BNN) becomes the low-cost high-accelerated inference machine for consumer electronics. However, except acceleration, power dissipation, area cost and reliability are also critical issues of AI accelerators. In safety-critical applications, the reliability issue becomes hard to trade and even more critical than cost and acceleration. Recently, people are understanding that only arithmetic codes can correct errors online. AN codes are effective and efficient arithmetic codes for improving the reliability of a BNN, but each class output requires an AN decoder. As a result, the power dissipation and associated area overhead not only highly in-crease the cost but also seriously affect the performance. In this paper, we propose a two-dimensional error-locating technique for sharing only a decoder. From experimental results, more than 97% of the logic elements and the associate power dissipation can be reduced.

PE07

Reliable Advanced Encryption Standard System Design with PUF-based Key Generators

Yi-Ting Lin, Shu-Yi Tsai, and Yu-Guang Chen
Department of Electrical Engineering, National Central University

Hardware Trojans and side channel attacks have become serious threats for modern cryptoprocessors. One of the attacker's goals is stealing key information for encryption and decryption algorithms. Therefore, it is important to find robust techniques to protect the key information. With the properties of robust, unique, easy to evaluate, difficult to replicate, and very difficult or impossible to predict, it has been shown that Physically Unclonable Function (PUF) is a promising cryptographic primitive to be a key generator. In this paper, we propose a reliable Advanced Encryption Standard (AES) system which applies Arbiter PUF (APUF) and Ring-Oscillator PUF (ROPUF) as key generators. We implement our AES system with PUFs on different FPGAs, and demonstrate the effectiveness of different PUF designs as key generators to protect the encryption circuit and decryption circuit of AES system. Moreover, we carefully study how the different place-and-route settings on FPGA influence the PUF behavior. Finally, we show the resource utilization and power analysis results on Xilinx Zynq-7000 SoC ZC702. Experimental show that our design not only can successfully provide reliable key to AES but also introduce acceptable design overhead.

PE08

A Systematic Region-Based Interleaving Reduction Approach for Concurrent Bug Testing

Kuo-Cheng Chin, Ren-Song Tsay, Hsin-I Wu, and Tzu-Hsuan Su
National Tsing Hua University

In this paper, we propose an effective concurrency bug testing approach that focuses on suspicious bug-causing code regions instead of indiscriminately testing the whole program. Additionally, with a simple loop heuristic, the region-based approach effectively avoids the state-explosion problem. It is highly efficient while guaranteeing to find any existing concurrency bugs in the specified code regions. We also devise an optimization scheme to reduce the number of interleavings to be examined to achieve maximum efficiency. Our method can conveniently identify bug-causing interleavings and hence significantly improve debugging efficiency. We have implemented the proposed approach and successfully tested on a few large application cases. The experimental results show that the approach can precisely identify bug sources and perform much more effectively than traditional approaches.

PE11

Exploring All Pairs of Circuit Nodes to Generate Combinational Hardware Trojan Detecting Patterns

Chien-Pu Lu and Hsing-Chung Liang
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Hardware Trojan (HT) invasion has become an important issue in the rapidly changing semiconductor field. In this paper, we propose a method to explore all possible pairs of circuit nodes and generate all required test patterns for detecting assumed combinational HT designs. Comparing to original stuck-at fault (SAF) patterns, we add only 1 to 8 multiples of additional patterns because of using pattern compression. These patterns can be prepared in very short time. In addition, experimenting on detecting those HT not assumed by our methods, we find that our patterns can have 43X stronger detectability than SAF patterns for the benchmark circuit s38584.

PE12

Applying Machine Learning to Custom-fix Timing Violations after Routing

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Timing aversion is a challenge in the physical design flow. However, timing analysis can only be performed accurately after the routing is completed, and in the process of fixing timing violations, the physical design tool can automatically converge most of the timing violations, but there are still some problems require a lot of time and cost for engineers to fix them. Therefore, our approach uses machine learning technology to extract the features of each critical path from the database in the post-route stage, and then conducts training to quickly repair the timing violation by the developed repair scheme.

PE13

PCB Component Copper Landing Pad Design Optimization

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As the density of electronic components increases in modern PCB designs, the adjustment of copper landing pads has become a complex and essential issue during PCB layout design stage. Common copper landing pad adjusting strategies are optimized by experienced PCB layout engineers. However, manual designs are error-prone and may suffer reliability degradation. In this paper, we propose an optimization framework to legalize copper landing pads via pad offset, pad cutting, and pad shrinking operations. The experimental results demonstrate the effectiveness to significantly reduce the manual task of PCB layout engineers for time and effort saving.

PE14

Recognizing Wafer Defects by Using Statistic Analysis of Geometric Features

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This paper proposes a method for judging defects on a wafer. We first analyze the five geometric parameters of defects on wafer bin maps. We statistically obtain the parameter intervals of various wafer defects. These intervals are used to analyze unknown wafer bin maps to determine possible wafer defects. Experiments show that our feature parameter intervals are accurate for judging wafer defects, which will help construct automatic wafer defect analysis system in the future.

Emerging Technology

PT01

Combining Low-Density Parity Check (LDPC) and Guessing Random Additive Noise Decoding (GRAND)

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Inevitably, there will have some errors when we sent the messages from the transmitter to the receiver created by the noise. To correct those errors, this paper introduces a universal decoding algorithm named Guessing Random Additive Noise Decoding (GRAND) and the details of the core module in the GRAND decoder. We tried different ways and different parameters to reduce the calculations, and also compared their performances.

PT02

iWalkSafe - Wearable Navigation Assistance for the Visually Impaired Based on Miniaturized Edge AI

Wei En Tsai[1], Kuo Cheng Chin[2], Borhan Lee[1], Wei Chung Chen[1], and Ren Song Tsay[1]
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We propose a computer vision-based, wearable navigation assistance based on a miniaturized AI model, utilizing the benefit brought by a specialized edge AI box. This study contributes to the literature in two ways. First, we implement a navigation system with high mobility, helping the visually impaired eliminate most of the common dangers in their daily lives. Second, we demonstrate how our previous work — a patented CNN miniaturization method — may be put into a critical application such as offline navigation assistance. The miniaturization technology enables the system with high mobility and low power consumption, with a negligible precision trade-off.

PT03

VLSI Implementation of the Traveling Salesman Problem Solver using Annealer Chip

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Quantum computing is one of the mainstream technologies in the future. However, due to temperature and cost constraints, this technology cannot be popularized. Thus many researchers have proposed "digital annealing" to replace it. Digital annealing is a new technique dedicated to solving large-scale, complex, and intractable quadratic unconstrained binary optimization (QUBO). By simulating the properties of quantum fluctuations, the optimal solution to the problem can be calculated. This study proposes an Ising model hardware architecture that can solve combinatorial optimization problems. Ising models can represent QUBO formulations with multiple solutions as polynomials, mapping to a fully connected Ising model architecture. According to the characteristics of digital annealing, the optimal solution can be obtained quickly. The proposed chip was implemented using a TSMC 90nm CMOS technology, the operating frequency is 50MHz, and the chip area is 3.24mm2.

PT04

VLSI Implementation of the Annealing Chip for Nurse Scheduling Optimal Problem

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In recent years, COVID-19 has changed everyone's life, and the world has been affected by its powerful contagion. Because of this, the allocation of medical resources is very important, especially the issue of nurses scheduling. The nurse scheduling problem is an optimization problem that can be solved using quantum computing. Quantum computing converts the problem into an Ising model and uses a quantum computer to find the optimal solution. This study proposes an annealed chip realized by VLSI, which can effectively solve the optimal solution of the Ising model by imitating the quantum computer. This work uses TSMC 90nm COMS to realize this chip, which achieves an operating frequency of 100MHz, a chip area of 2.15mm2 , and maximum power consumption of 15.38mW. Compared with chips in the existing works, this paper achieves a low-power, high-speed chip implementation.

PT05

A Low-Cost Way to Pick the Sick Image in Sick OCT Volume

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We propose to solve the problem of noise images in sick volume by using a screening process. In order to find out the noise image in the FEMH dataset by using the Duke dataset, we use CycleGAN to convert the image style of the FEMH dataset into the image style of the Duke dataset, by the above way, the success rate is increased from 76% to 83%.

PT06

Detecting Anomalous Lane-Changing Decisions for Connected and Autonomous Vehicles

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The goal of this work is to detect if a lane-changing decision and the sensed or received information are anomalous. We develop three anomaly detection approaches based on deep learning, where all of them do not need anomalous data nor lateral features so that they can generally consider lane-changing decisions before the vehicles start moving along the lateral axis. They achieve at least 82% and up to 93% F1 scores against anomaly on data from Simulation of Urban MObility (SUMO) and HighD. We also examine system properties and verify that the detected anomaly includes more dangerous scenarios.