Oral S15

Advanced Circuit Techniques for RF/mm-Wave Applications

Date/Time 8/4 (四) 14:30-15:30

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S15.1 14:30 – 14:42

A 187 μW Multi-Mode Wake-Up Receiver Achieving –97 dBm Via a Balun LNA

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This paper presents an energy efficiency wake-up receiver (WuRx) with a balanced-to-unbalanced low noise amplifier (balun LNA) to achieve high sensitivity. Based on an injection-locked oscillator (ILO) and an envelope detector, the prototype WuRx provides the capabilities of reliable demodulation for on-off keying (OOK), binary frequency shift keying (BFSK), and differential binary phase-shift keying (DBPSK) demodulation schemes. A 187 μW 433 MHz multi-mode WuRx is implemented in a 0.18-μm CMOS process. For a data rate of 200 kbps and packet error rate (PER) of 10-1 with false alarm rate (FAR) < 10-3/s, the receiver achieves sensitivities of–97/–96/–94 dBm under the OOK/BFSK/DBPSK demodulation schemes, respectively.

S15.2 14:42 – 14:54

A Type-3 FMCW Radar Synthesizer with Wide Frequency Modulation Bandwidth

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This work presents a 5-GHz frequency-modulated continuous wave signal generator (FMCW). The presented circuit aims to generate a wider frequency modulation bandwidth at a low center frequency that grants a significant advantage in saving power. Utilizing a fractional-N phase-locked loop (PLL)-based synthesizer with a 50-MHz reference frequency as the FMCW generator, the synthesizer modulates the carrier frequency across a range of 700 MHz. A Type-3 architecture with a switchable polarity is embedded to improve the linearity around the chirp turning-around points (TAPs) and switching-band points (SBPs). Switching Band Control (SBC) circuit and Multi-varactor LC Voltage Control Oscillator (MV-VCO) are proposed as an efficient method to increase the modulation range so that the FMCW signal generator can achieve 21.43-cm resolution in distance detecting. Fabricated in a TSMC 40-nm 1P10M CMOS technology, the proposed generator consumes 3.3 mW power and occupies 0.497 mm2 die area. The measured root-mean-square (rms) frequency error of the generated triangle chirp over 1.15 ms period is 625 kHz.

S15.3 14:54 — 15:06

A 17-21 GHz Current-Folding Frequency Tripler With >36-dBc Harmonic Rejection and 190.8-dB FoM in 90-nm CMOS

Chun-Hung Lin and Ching-Yuan Yang
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A frequency tripler (FT) using a current-folding technique to achieve inherently nonlinear operation is presented. A built-in VCO generates the fundamental signal, and the proposed current-folding stage converts the fundamental input into the triple-frequency output, which is injected into a bandpass stage for harmonic suppression. Fabricated in 90-nm CMOS technology, the measured FT features 36 to 43-dBc harmonic rejection from 17.5 to 21 GHz (18.2% FTR), while consuming 3.5 mW only from 1.2-V supply. The measured phase noise (PN) of the VCO and the FT are -112.5 and -102.8 dBc/Hz at 1-MHz offset, respectively. Furthermore, the achieved figure-of-merit (FoM) of the FT are -180.52 and -190.87 dB at 1-MHz and 10-MHz offset, respectively. To the best of our knowledge, the proposed FT achieves outstanding performance on both harmonic rejection and FoM among the state-of-the-art multipliers.

S15.4 15:06 — 15:18

Simultaneous Noise and Input Matching for W-Band LNA Using Parallel Coupled Transmission Lines

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This proposed low-noise amplifier (LNA) for W-band applications adopts four stages of common source topology. The implement of the chip was fabricated by using TSMC 90-nm CMOS GUTM 1P9M process. With the parallel-coupled transmission lines between the voltage bias of gate terminal and the degenerative source terminal, this structure is applied to optimize among the specifications of noise, input matching and gain. From the measurement results, the peak gain is 13.15 dB at 73 GHz; the minimum noise figure is 4.83 dB at 77.5 GHz; input P1dB is –7.3 dBm at 78 GHz, and the corresponding IIP3 is –1.1 dBm. The chip area is 0.730×0.588 mm2, and the total power consumption is 28.14 mW under 1.2-V supply.

S15.5 15:18 — 15:30

A 94 GHz Low-Power Down-Conversion Mixer With Negative-R Gain Enhancement

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A W-band single-balanced mixer is designed and fabricated in 40 nm digital CMOS technology. The mixer down-converts the 94 GHz rf input to the 10 GHz IF output. The entire circuit consumes dc power of 6.6 mW with the supply voltage of 1 V, while the core circuit consumes only 2.8 mW. The measured peak conversion gain achieves 4.3 dB at 94 GHz. The input 1-dB gain compression point (iP1dB) is -13 dBm. The core circuit occupies a small area of only 0.22 mm2