Oral S14

Emerging Algorithms and Future Computing Technologies

Date/Time 8/4 (四) 14:30-15:30

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S14.1 14:30 – 14:42

Partial Equivalence Checking of Quantum Circuits

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Equivalence checking of quantum circuits is an essential element in quantum program compilation, in which a quantum program can be synthesized into different quantum circuits that may vary in the number of qubits, initialization requirements, and output states. Verifying the equivalences among the implementation variants requires proper generality. Although different notions of quantum circuit equivalence have been defined, prior methods cannot check observational equivalence with respect to measurement between two quantum circuits whose qubits are partially initialized, which is referred to as partial equivalence. In this work, we devise algorithms for partial equivalence checking. Experiments demonstrate the generality of our method in checking quantum circuits whose partial equivalence cannot be verified by prior approaches and the effectiveness of our method in subsuming prior more restricted equivalence checking. Our result may unleash the optimization power of quantum program compilation to take more aggressive steps.

S14.2 14:42 – 14:54

Bearing Fault Diagnosis by Using Exponential Power Entropy and a Decision Threshold for Artificial Neural Network

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Rotating machinery is used in a variety of industries including petroleum, automotive and food processing, etc. which uses bearings to reduce the friction between the moving parts. Besides, bearings are prone to wear due to a variety of conditions such as speed variations, heavy loads, and lengthy periods of operation. Therefore, real-time monitoring and diagnosis of bearing faults will improve safety, avoiding unplanned downtime and lowering the cost. Condition-based maintenance (CbM) is usually employed to observe the faults that arises in a healthy condition of the machine, running by gathering sensing vibration signals. However, the massive sensing data increase the challenge to analyze the fault signal will result in high computing time. To solve this problem, we propose an Exponential Power Entropy (EPE)-based feature extraction and selection approach to minimize the computing data and used a feed-forward neural network for fault classification with a proposed decision threshold score to improve the prediction accuracy. Compared with the conventional approaches, the proposed method not only reduce the computing time by 64.8% but also increase the accuracy of fault diagnosis up to 99.2%.

S14.3 14:54 — 15:06

Edge AI Implementation for Heterogeneous Images Semantic Segmentation

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The deep convolutional neural network-based semantic segmentation needs large-scale computations and annotations for data training to reach real-time inference speeds. The heterogeneous image semantic segmentation method extracts the features of visible and thermal images separately. We designed an efficient architecture with the multi-hybrid-autoencoder and decoder for Faster Heterogeneous Image (FHI) Semantic Segmentation. The proposed architecture has fewer layers resulting in lower parameters, higher inference speed. The specialty of this architecture is the discrete autonomous feature extraction framework for RGB image and Thermal (T) image inputs with individual convolutional layers. Later, we combined the 4-channels (RGBT) convolution features to reduce computational complexity and robust the model performances. The proposed FHI-Unet semantic segmentation model experimented on NVIDIA Xavier NX edge AI platforms with standard accuracy under the real-time inference requirement. The proposed FHI-Unet model has fastest real-time inference of 83.39 frames per second on edge AI implementation on the Multi-spectral Semantic Segmentation Dataset compared with the existing works.

S14.4 15:06 — 15:18

Polar Code Belief Propagation Decoder with Stage Stopping Scheme under Round Trip Scheduling

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Capacity-achieving polar codes have grown attention in recent years, and the belief propagation (BP) algorithm is one way to decode them. With the help of Min-sum approximation and G-Matrix early termination schemes, it has been proven that complexity and computation can be further reduced without significant performance loss. Although G-Matrix early termination is a strong stopping criterion, there are still some redundant cycles that need to be reduced. In this paper, a stage-stopping BP algorithm with round-trip scheduling is applied to reduce the redundant computation. Different thresholds for different SNR regions are simulated to seek the proper combination. The results show that threshold=3 is suitable for the SNR region in{1,1.5,2,2.5,3} (dB), and threshold=3/3.5 can be selected for lower computation or better performance in {3.5} (dB). As for the high SNR region in {4,4.5,5} (dB), threshold=5.5 is suitable for better performance.

S14.5 🕓 **15:18 — 15:30**

Toward Optimal Topology Generation and Efficient Radius Selection for Parallelism-Aware Wavelength-Routed Optical Networks-on-Chip Design

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The wavelength-routed optical network-on-chip (WRONoC) emerges as a promising solution for multi-core system communication, providing high-bandwidth, high-speed, low-power, and low-latency transmission. However, as the number of cores in a WRONoC increases, some wavelength-routed optical network-on-chip (WRONoC) topologies could be infeasible with bandwidth and crosstalk constraints if bit-level parallelism is not considered during topology generation. In previous work, the parallelism was optimized only for the radius selection of microring resonators but not for topology generation. Further, existing parallelism-aware WRONoC designs are too time-consuming to handle the current design sizes efficiently. To remedy these drawbacks, we present a parallelism-aware WRONoC design flow to optimize parallelism in topology generation and radius selection. The proposed design flow guarantees to generate a parallelism-optimal topology for full connectivity; and parallelism-optimal topology for customized connectivity if the netlist meets certain conditions. Compared with the state-of-the-art methods, experimental results show a 31.6% improvement in parallelism. Besides, the proposed radius selection method can significantly reduce runtime without performance loss.