Oral S13

Digital Signal Processing ICs, Image/Visual & Multimedia Systems

Date/Time 8/4 (四) 14:30-15:30

Chair(s) 李佩君教授 / 國立臺灣科技大學電子工程學系
李宇軒教授 / 元智大學電機工程學系

S13.1 14:30 – 14:42

Modularized and Extensible Convolution Cell Design and Chip Implementation for AI Accelerator

Wei-Hsuan Chang and Chung-Bin Wu
National Chung-Hsing University

This paper proposes a modularized and extensible Convolution Cell for neural network accelerators. Each unit of convolution cell is composed of 72 PEs and can be arbitrarily expanded to above 72xN up to 2160 PEs. The Convolution Cell is designed to be quickly reconfigured into application requirements under certain memory size and hardware specifications. In addition, the Convolution Cell can support two convolution operation modes, 1x1 and 3x3, can be adapted to the network architecture of the Yolo series. In FPGA implementation, one Convolution Cell are configured to reach 7.69GOPS/W and two Convolution Cell to reach 15.22GOPS/W. In 40nm Chip implementation, according to analyzing area into million gate equivalent (MGE) and energy efficiency, one Convolution Cell can reach 66.5 GOPS/MGE and 316.4 GOPS/W.

S13.2 14:42 – 14:54

Architecture Implementation on FPGA for CNN with Gabor Feature Extraction

Yu-Wen Wang
Department of Electrical Engineering, National Cheng Kung University

This paper implements a hardware design that can calculate the 2-dimensional convolution with specific Gabor filters onto a Field Programmable Gate Array (FPGA). As a popular algorithm in the field of computer vision today, Convolutional Neural Network (CNN) requires a huge amount of computation and therefore requires hardware and special algorithms to accelerate. For reducing the number of additions and multiplications, we use the Eigen-transformation approach to transform the 16 Gabor filters into the 16 transformed filters with a high degree of symmetry and then pre-add the input pixels corresponding to the position of the repeated coefficients. We analyze the four models of processing units for the transformed filter bank proposed by the previous work in our lab and use the Xilinx XUPV5-LX110T Evaluation Platform for prototyping. Finally, we use the Xilinx Chipscope as an integrated logic analyzer for verification.

S13.3 🕓 **14:54 — 15:06**

A Parallel-Process Auto-Clear Time-to-Digital Converter Chip Integrated with SPAD Sensors for a LiDAR System

Yi-Chen Hsieh, Ching-Hwa Cheng, and Don-Gey Liu
Department of Electronic Engineering, Feng Chia University

The proposed design proposes to perform parallel computing processing on the two groups of TDCs, to improve the calculation speed of the overall TDC, reduce its death time, and maintain high resolution capability at the same time. And integrating SPAD and TDC on the same chip can speed up the TDC input and SPAD output transmission to reduce the delay time of signal transmission. The proposed design integrates the front-end SPAD optical sensor and TDC circuit, and adopts the TSMC-T18HVG2 process. The reference clock frequency is 100MHz. TDC shortest dead time is 20ns, resolution is 100ps, measurement range can reach 337.5 meters, and the chip area is 2.5 mm2. Two TDCs can operate at the same time; the speed of data transmission will be greatly improved to bringing a high-performance LiDAR system.