Oral S12

Power Management & Readout IC

Date/Time	8/4 (四) 13:30-14:30
Chair(s)	陳柏宏教授 / 國立陽明交通大學電機工程學系 陳景然教授 / 國立臺灣大學電機工程學系

S12.1 13:30 — 13:42

A V3-Controlled Buck Converter with Pseudo-Current Sensing Technology

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This paper presents a V3-Controlled Buck Converter with Pseudo-Current Sensing Technology. The proposed converter achieves fast transient response and a wide output voltage range. The proposed buck converter is fabricated with TSMC 0.18μm 1P6M CMOS technology, and the chip area is 1.052 mm× 0.942 mm. The measured results show that the output voltage is 1.6V, the load current changes from 50mA to 500mA, and the transient response from 50mA to 500mA is 2μs and 2μs, respectively. When the load current is 400mA, the maximum power efficiency is 93.2%.

S12.2 13:42 — 13:54

An Adaptive 2nd-Order Delta-Sigma-Modulation Buck Converter with Transient-Accelerated-Circuits

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This paper presented an adaptive 2nd-order continuous-time delta-sigma-modulation (CT-DSM) current-mode controlled buck converter with transient-accelerated-circuits that features an integral loop filter with a superiority of oversampling and noise shaping for effective spurious-noise reduction. In addition, the Transient-Accelerated-Circuits (TAC) use dynamic-slope generator and current-sensor to speed up the transient response. Then, the proposed buck converter preserves a low spurious noise and fast transient response. The proposed buck converter is fabricated in TSMC 0.18um 1P6M CMOS processes with a chip area of 1.19mm × 1.19mm. The measurement results show that the transient recovery times are 2.7μs and 3.1μs, and the undershoot and overshoot voltages are 22mV and 24mV, when the load current changes from 50mA to 500mA and from 500mA to 50mA. The output spectrum with signal to noise ratio is 77dB was obtained across all sampling frequencies. The peak power efficiency is 94.88%, when the load current is 400mA and output voltage is 2V.

S12.3 🕓 13:54 — 14:06

An Adaptive On-Time Buck Converter with New Integral Current-Sensing and Dynamic Slope Compensation Techniques

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An adaptive-on-time buck converter with new integral current sensing and dynamic-slope compensation techniques is presented in this paper. First, the adaptive on-time controlled scheme is adopted, which is based on the techniques of the on-time controlled by input voltage feedforward and output voltage feedback, by using this scheme, a relatively constant switching frequency can be obtained. Second, the proposed converter uses the integral current-sensing circuit with the linearized input-stage OTA to sense the inductor current, which increases the bandwidth of the converter's closed-loop gain and will speed up the converter's transient response. Third, the converter uses the dynamic-slope compensation techniques to eliminate subharmonic oscillation when the duty cycle is greater than 50%. The proposed converter is designed and fabricated in TSMC 0.18μm 1P6M CMOS process, and the chip area is 0.998mm × 0.949mm. When the load current changes from 50mA to 500mA and 500mA to 50mA, the transient responses are 2.6us and 2.5us, respectively, and the maximum efficiency is 93.2%.

Keywords: Buck converter, Adaptive-On-Time (AOT), Dynamic-Slope Compensation, Integral Current-Sensing

S12.4 🕓 14:06 — 14:18

A Cross-Correlation-Based Time-of-Flight Design for Chaos Lidar Systems

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This work presents a time-of-flight circuit design for chaos lidar systems. It is implemented by a mixed-signal structure, with 1-bit digitization and a multiplier-and-integrator array to calculate the cross-correlation between the two signals to estimate the time difference and the corresponding distance. With an off-chip tunable low-pass filter, the ranging accuracy and detection distance can be adjusted more effectively and flexibly.

This work is implemented in CMOS 90-nm process. At the sampling rate of 5 GS/s, the measurement results demonstrate that the maximum ranging error is 3.38 cm and 1-sigma is 1.97 cm in the ranging range of 7.4m. With a pulse width of 100ns and a repetition interval time of 50 μs, this work consumes 113 mW under 1-V supply.

S12.5 14:18 — 14:30

A VRO-based TDC for a light sensor application

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A vernier ring oscillator (VRO) based time to digital converter (VRO-based TDC) proposes for the timing resolutions of the coarse-tuning stage (CTS) and the fine-tuning stage (FTS) have a proportional relationship under the process, voltage and temperature (PVT) variations. In the input range, the CTS can be flexibly to extend the bit number for a wide input range. The timing resolutions of CTS and FTS are defined by the rise time and the fall time. Therefore, the timing ratio between CTS and FTS is a constant under the PVT variations. This 14-bit TDC was fabricated in a 0.18 μm standard CMOS process and the core area of 62×199 μm2. The measured timing resolution of the proposed VRO-based TDC was 125 ps and the input range was from 10 ns to 200 ns. The DNL and INL were less than ±1 LSB and ±1.64 LSB, respectively. The proposed VRO-based TDC is also integrated with a light sensor for internet of things (IoT) applications.