Oral S09

Data Converters and Clock Generator

Date/Time 8/4 (四) 11:00-12:00

Chair(s) 彭朋瑞教授 / 國立清華大學電機工程學系
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S09.1 11:00 – 11:12

A 400KS/s 62.6pJ/c.-s 10-bits Column-Parallel Hybrid ADC Using Self-Adaptive Charge-Injection Cell and Single-Slope Conversion

Min Ruei Wu and Chih Cheng Hsieh
Department of Electrical Engineering, National Tsing Hua University

This work presents a column-parallel hybrid ADC using self-adaptive (SA) charge-injection (CI) cell and single-slope (SS) conversion for CMOS image sensor (CIS) applications. The proposed scheme solves the speed bottleneck in conventional SS ADC without the need of high frequency clock. To satisfy the column-to-column matching requirement in CIS readout, we proposed a SA ci-cell that achieves high linearity performance without calibration. The prototyped 10-bits column-parallel ADC is fabricated in 40nm 1P9M CMOS and achieves a sampling frequency of 400KS/s with only 40MHz counting clock with an energy efficiency FoMw of 62.6pJ/c.-s.

S09.2 11:12 – 11:24

A 77.16 dB SNDR 10MHz Bandwidth Continuous Time ΔΣ ADC with VCO-Based Quantizer

Guan-Yu Chen and Zhen-Jie Hong
Department of Electronic Engineering, Feng Chia University

This paper reports a continuous-time (CT) third-order delta-sigma (ΔΣ) analog-to-digital converter (ADC) in a 0.18 μm CMOS process for ultrasound testing over a 10 MHz signal bandwidth with a 1GHz sampling rate (Fs). There are two critical technologies are implemented to lower the power dissipation of this ADC. First, the conventional quantizer based on the flash ADC is replaced with a voltage-controlled oscillator (VCO)-based quantizer which works like an integrator providing a first-order noise shaping. This additional noise shaping help to save an integrator and lower the power. Another reason to choose a VCO-based quantizer is due to its implicit clocked averaging (CLA) can save additional dynamic element matching (DEM) circuits to reduce the mismatch of a digital-to-analog converter (DAC). Second, with such high Fs (1GHz), the OPA is adopted with active feedforward compensation to improve the unit gain bandwidth (UGB). It is an efficient way to enhance the UGB and does not cost too much power consumption simultaneously.

The prototype ADC achieves a 79.9 dB signal-to-noise ratio (SNR), 77.16 dB signal-to-noise and distortion ratio (SNDR), and 79.3 dB dynamic range (DR), respectively, over a 10 MHz signal bandwidth with a 1GHz sampling rate. The whole ADC total consumes 30.7 mW of power from a 1.8 V power supply.

S09.3 11:24 — 11:36

FPGA Multichannel Digital to Time Converter based on Multidimensional Delay

Tai-Sen Lin, Jane Chen, and Poki Chen
Department of Electronic and Computer Engineering, National Taiwan University of Science and Technology

This paper presents a precise multichannel digital-to-time (DTC) converter, or digital pulse generator, based on multidimensional delay array. It is also proposed to further extend FPGA applications into the analog domain. Multidimensional delay array is composed of a delay matrix and a phase-locked loop (PLL) with phase shifting so that output phases are uniformly distributed within the reference clock period. For the proof of concept and performance evaluation, the proposed multichannel DTC based on multidimensional delay array is implemented and the achieved fine stage resolution is as high as 2 ps. The differential nonlinearity (DNL) and integral nonlinearity (INL) of this architecture is measured to be -4.7 ~ 6.7 LSB and -4.8 ~ 5.8 LSB respectively.

S09.4 11:36 — 11:48

A 12-bit 100KS/s SAR ADC with Split Capacitor Array DAC and Offset Calibration

Yun-Yen Huang and Chung-Chih Hung
Department of Electrical and Computer Engineering, National Yang Ming Chiao Tung University

This paper presents a 12-bit 100KS/s successive approximation register (SAR) analog-to-digital converter (ADC) in TSMC 0.18-μm process. To reduce the switching energy and save the total capacitance, a hybrid switching procedure with split capacitor array DAC is applied. The hybrid switching procedure combines two concepts of one side switching instead (OSSI) and higher bits switching instead (HBSI). Besides, a dynamic comparator with adjustable capacitor calibration to achieve low offset is used. With 1.8V supply voltage and 100K sampling rate, simulation results achieve 73.15dB signal-to-noise-and-distortion-ratios (SNDR) which lead to 11.86 effective number of bits (ENOB) at 49.97k input frequency. Its power consumption is 5.04-μW and figure-of-merit (FOM) is 13.5 fJ/conversion-step.

S09.5 11:48 — 12:00

A 197-ppm/°C 2.5-GHz Low-Voltage Oscillator Using Frequency-Locked Loop in 180-nm CMOS

Tsung-Ying Chen and Ching-Yuan Yang
National Chung Hsing University

In the paper, we present a low-voltage oscillator using the frequency-locked loop (FLL) circuit in 0.18μm CMOS process. With employing the FLL, The output frequency depends on passive components and divider ratio to reach low temperature variation and frequency programmable ability. Operation at 2.5 GHz, the temperature stability for the oscillator is about 197.76 ppm/°C from 0°C to 100°C and line sensitivity is 5.91 %/V from 0.9V to 1.1V.