Oral S08

Advances in Modern EDA Methods and Technologies

Date/Time 8/4 (四) 11:00-12:00

Chair(s) 陳盈如教授 / 國立成功大學電機工程學系
鄭維凱教授 / 中原大學資訊工程學系

S08.1 11:00 — 11:12

Keeping Deep Lithography Simulators Updated: Graph-Based Smart-Sampling Schemes for Active Learning

Hao-Chiang Shao[1], Kuo-shiuan Chen[2], Hsing-Lei Ping[2], Weng-Tai Su[2], Chia-Wen Lin[2], Shao-Yun Fang[3], Pin-Yian Tsai[4], and Yan-Hsiu Liu[4]
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Learning-based pre-simulation (i.e., layout-to-fabrication) models have been proposed to predict the fabrication-induced shape deformation from an IC layout to its fabricated circuit. Such models are usually driven by pairwise learning, involving a training set of layout patterns and their reference shape images after fabrication. However, it is expensive and time-consuming to collect the reference shape images of all layout clips for model training and updating. To address the problem, we propose two active-learning strategies for sampling novel layouts beneficial to the model update process. Given a set of predefined newly-desgined novel layout patterns, the proposed methods aim to sample a reduced amount of representative layouts most worthy to be fabricated for acquiring their ground-truth circuit shapes. Experiments demonstrate our active-learning strategies' ability in selecting representative novel layouts for keeping a learning-based pre-simulation model updated.

S08.2 11:12 — 11:24

TCG-based Warpage-aware Floorplanning for Heterogeneous Integration

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In modern heterogeneous integration technologies, chips with different processes and functionality are integrated into a package with high interconnection density and large I/O counts. Integrating multiple chips into a package may suffer from severe warpage problems caused by the mismatch in coefficients of thermal expansion between different manufacturing materials, leading to deformation and malfunction in the manufactured package. To our best knowledge, the industry is eager to find a solution for the warpage optimization. In this paper, we propose the first warpage-aware floorplanning algorithm for heterogeneous integration. We first present an efficient qualitative warpage model for a multi-chip package structure based on Suhir's solution, more suitable for optimization than the time-consuming

finite element analysis. We then propose three perturbations for the transitive closure graph floorplan representation to optimize the warpage more directly and can thus speed up the simulated annealing process. Finally, we develop a force-directed detailed floorplanning algorithm to further refine the results by utilizing the dead spaces. Experimental results demonstrate the effectiveness of our warpage model and algorithm.

S08.3 11:24 — 11:36

Thermal-Aware Chiplet Placement on Interposer-Based 3D ICs via Thermal Weighted Nets and Refinement

Hong-Wen Chiou, Yu-Teng Chang, Ting-Yu Cheng, and Yu-Min Lee
Institute of Communications Engineering, National Yang Ming Chiao Tung University

Up to now, researches for the chiplet placement of interposer-based 3D ICs focus on the minimization of wire lengths. This work aims to simultaneously consider the issues of wirelength and thermal effect in chiplet placement. We introduce the concept of thermal weighted net that is applied to the advanced Branch-and-Bound method and develop a refinement method to improve the placement result for reducing the maximum temperature. Experimental results show that they can satisfy the temperature constraint at only sacrificing most of 5.88% total wirelength.

S08.4 11:36 — 11:48

Improving Pin Accessibility of Standard Cells under Power/Ground Stripes

Pei-Sheng Lu and Rung-Bin Lin
Yuan Ze University

This paper presents an approach to improving pin accessibility of standard cells under power/ground (P/G) stripes. Two strategies are used. First, hard-to-access cells located under M3 P/G stripes are swapped with easily accessible cells in close proximity. Second, filler cells are added at some places under P/G stripes to push hard-to-access cells away from P/G stripes. Experimental results show that cell swapping can reduce DRC violations by 86% while averagely maintaining timing performance. Filler insertion can reduce DRC violations by 80% but less effective in maintaining timing performance.

S08.5 🕓 **11:48 — 12:00**

Timing-Critical Path Analysis in Circuit Designs Considering Aging with Signal Probability

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Aging is an important determinant for the reliability of circuit designs. and has been addressed by a number of protection techniques based on static timing analysis (STA). The timing reported by STA, however, is often too optimistic without considering the functional behavior of the circuit. Furthermore, signal probability has also been found to be a significant factor in the aging effect. As such, we present in this paper a timing-critical path analysis that takes function and aging into account as well as signal probability. Functional timing analysis (FTA) eliminates the false paths and generates more accurate timing. Furthermore, machine learning can be used to build models for predicting the timing of each cell for various aging lifetimes and signal probabilities. Experimental results indicate that there can be a difference of up to 6% on path delay between STA and FTA. The path ranks also differ for most of the benchmark circuits after considering aging with signal probability, resulting in the delay differences of up to 7%. In conclusion, it is necessary to consider function, aging, and signal probability simultaneously when analyzing timing-critical paths in a circuit design.