Oral S06

Sensor Interface Circuits

Date/Time 8/3 (三) 14:30-15:30

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S06.1 14:30 – 14:42

A Buffer Amplifier with Self-Adapted Current for Biomedical Applications

Zu-Jia Lo, Yuan-Chuan Wang, Yun-Jie Huang, Ren-Yong Hung, Yi-Heng Wu, and Sheng-Yu Peng
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A power-efficient amplifier with self-adaptive supply current is proposed for biomedical signal buffering application. Without extra sensing and control circuitries, the current consumption of the proposed amplifier increases spontaneously when the input signal is fast or large, achieving a high slew rate. The supply current dwindles back to the low quiescent level autonomously when the output voltage reaches equilibrium. Therefore, the proposed ACABA is power-efficient and suitable for processing physiological signals. A prototype version has been designed and fabricated in a 0:35 μm CMOS process occupying an area of 0:151 mm2. When loaded by a 10 pF capacitor, it consumes 3 μW to achieve a unity-gain bandwidth of 100 kHz, THD of - 60 dB under 1:8Vpp input amplitude, and a slew rate of 7:86V/μs.

S06.2 14:42 – 14:54

A Low-Power Sensing System of VEGF Concentration with Monolithic Electrodes and An All-Digital Sub-Sampling Delay-Locked Loop

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A low-noise sensing system using sub-sampling technique to suppress the interface noise is presented. The CMOS MEMS capacitive transducer is integrated on the same chip for the point-of-care (PoC) applications. The biomarker is vascular endothelial growth factor (VEGF). The proposed sensing system converts the capacitance variations caused by the VEGF concentration at the transducer into digital codes with a low-power SAR-assisted time-to-digital converter (TDC). CMOS MEMS interdigitated electrodes are adopted as the transducer. Post-process etching and Au plating are implemented on the surface of the electrodes. Experimental results show that a capacitive resolution of 28.3 fF and a sensing range of VEGF concentration from 1 to 1000 pg/ml are achieved. The power consumption of the sensing system is merely 60.65 μW. The FOM of the proposed capacitance-to-digital converter (CDC) is 0.76 pJ/conv.-step.

S06.3 14:54 — 15:06

A 53mK-NETD Low Power ROIC for 80*60 Microbolometer CMOS Thermal Image Sensor with Ultra High Dynamic Range

Hsin Yu and Chih-Cheng Hsieh
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This paper presents an 53-mK NETD 18-bits Microbolometer ROIC using current-mode folding-integration and hybrid ADC. By using the folding integration operation, wide dynamic range and the tolerance to pixel non-uniformity can be achieved without costing additional power and chip area. Moreover, The proposed coarse fine hybrid ADC achieves the integration capacitance (Cint) mismatch immunity. The prototyped ROIC was fabricated in 0.18 um CMOS process with chip area of 2.28x2.28 mm^2, and it consists of 80x60 pixel array with a pitch of 18 um. The final noise equivalent temperature difference (NETD) is 53-mK, and the power consumption is 12.8mW.

S06.4 15:06 — 15:18

A High-Sensitivity CMOS-MEMS IL-6 Sensing System with an All-Digital Phase-Lock-Loop-Based Capacitance-to-Digital Converter

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A high-sensitivity electrochemical sensing system integrating the CMOS MEMS electrodes and the readout circuits on a single chip is presented. In-house wet etching post process is used to release the MEMS structure. The Interleukin-6 (IL-6) concentration is detected through the capacitance variations using the proposed vertical interdigitated capacitive MEMS transducer and then digitized by an all-digital phase-locked-loop (ADPLL) based capacitance to digital converter (CDC). Parasitic capacitance and noise are greatly reduced owing to the whole system integration on a single chip. The capacitive MEMS transducer is inserted in the oscillator of the ADPLL. When the sensing capacitance changes, frequency drift will be produced. The ADPLL will force the oscillation frequency to track the reference frequency and produce the digital output codes. Moreover, the proposed CDC can cancel the errors result from post process variations, parasitic capacitance and circuit delays. The sensitivity and sensing range of the proposed sensing system are 0.8 nF/ppm and 0~1000 pg/ml, respectively. The prototype chip is fabricated in TSMC 0.18 μm 1P6M CMOS process with an area of 1.2*1.2 mm2, 1.5mW power consumption and a FoM of 31.65 pJ/step.

S06.5 🕓 **15:18 — 15:30**

A Switched-Capacitor Based Acoustic Feature Extraction for Voice Activity Detection

Meng-Ju Chiang and Soon-Jyh Chang
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This paper presents a low-power acoustic feature extraction (AFE) for voice activity detection (VAD). It adopts analog signal processing to extract voice features. With the low feature rate, it is more power efficiency compared to the digital AFE. To overcome the issues of PVT variations, use the switched-capacitor (SC) bandpass filter (BPF) in this work with the op-amp sharing technique to reduce the power consumption. In addition, the chip is free from off-chip calibration. Measurement results of AFE chip, fabricated in a 0.18 μm CMOS process, has a core area of 0.65 mm2 and consumes 2 μW in 1.8 V supply voltage. It achieves an averaged 92%/97% speech/non-speech hit rate at a 3dB signal-to-noise ratio (SNR) with 32 ms latency, which corresponds to all the specifications of practical application.