Oral S02

Cutting Edge EDA Research

Date/Time 8/3 (三) 13:30-14:30

Chair(s) 麥偉基教授 / 國立清華大學資訊工程學系

S02.1 13:30 – 13:45

Compatible Equivalence Checking of X-Valued Circuits

Yu-Neng Wang[1], Yun-Rong Luo[1], Po-Chun Chien[2], Ping-Lun Wang[1], Hao-Ren Wang[2], Wan-Hsuan Lin[1], Jie-Hong Roland Jiang[1,2], and Chung-Yang Ric Huang[1,2]
[1]Department of Electrical Engineering, National Taiwan University
[2]Graduate Institute of Electronics Engineering, National Taiwan University

The X-value arises in various contexts of system design. It often represents an unknown value or a don't-care value depending on the application. Verification of X-valued circuits is a crucial task but relatively unaddressed. The challenge of equivalence checking for X-valued circuits, named compatible equivalence checking, is posed in the 2020 ICCAD CAD Contest. In this paper, we present our winning method based on X-value preserving dual-rail encoding and incremental identification of compatible equivalence relation. Experimental results demonstrate the effectiveness of the proposed techniques and the outperformance of our approach in solving more cases than the commercial tool and the other teams among the top 3 of the contest.

S02.2 13:45 – 14:00

Routability-driven Global Placer Target on Removing Global and Local Congestion for VLSI Designs

Jai-Ming Lin[1], Chung-Wei Huang[1], Liang-Chi Zane[1], Min-Chia Tsai[1], Che-Li Lin[2], and Chen-Fa Tsai[2]
[1]Department of Electrical Engineering, National Cheng Kung University
[2]Department of Physical Design Service, Global Unichip Corporation

Cell placement remains a big challenge in the modern VLSI design especially in routability. Routing overflow may come from global and local routing congestion in a placement. To target on resolving these problems, this paper proposes two techniques in a global placement algorithm based on an analytical placement formulation and the multilevel framework. To remove global routing congestion, we consider each net as a movable soft module and propose a novel congestion-aware net penalty model so that a net will receive a larger penalty if it covers more routing congested regions. Therefore, our placement formulation can be more easier to move nets away from routing congested regions than other approaches and has less impact on wirelength. In addition, to relieve local congestion, we propose an inflation technique to expand the area of a cluster according to its internal connectivity intensity and routing congestion occupied by the cluster. The experimental results demonstrate that our approaches can get better routability and wirelength compared to other approaches such as NTUplace4h, NTUplace4dr, and RePlAce.

S02.3 14:00 — 14:15

A Complete PCB Routing Methodology with Concurrent Hierarchical Routing

Shih-Ting Lin[1], Hung-Hsiao Wang[1], Chia-Yu Kuo[1], Yolo Chen[2], and Yih-Lang Li[1]
[1]National Yang Ming Chiao Tung University
[2]Wistron NeWeb Corporation

Trends in high pin density and an increasing number of routing layers complicate printed circuit board (PCB) routing, which is categorized as escape and area routing. Traditional escape routing research has focused on escape routing but has not considered the quality of area routing among chip components at the same time. In this work, we propose a complete PCB routing methodology, including simultaneous escape routing (SER), post-SER refinement, and gridless area routing. The SER completes the layer assignment of all nets and produces an escape order ensuring suitable escape and area routing on each layer. Length-matching constraints and differential pair routing are satisfied in each stage of the routing flow. The experiment results indicate that the proposed PCB routing method can complete routings for seven commercial PCB designs, whereas the commercial PCB tool cannot complete any of them.

S02.4 14:15 — 14:30

An Optimal Algorithm for Splitter and Buffer Insertion in Adiabatic Quantum-Flux-Parametron Circuits

Chao-Yuan Huang, Yi-Chen Chang, Ming-Jer Tsai, and Tsung-Yi Ho
Department of Computer Science, National Tsing Hua University

The Adiabatic Quantum-Flux-Parametron (AQFP), which benefits from low power consumption and rapid switching, is one of the rising superconducting logics. Due to the rapid switching, the delay of the inputs of an AQFP gate is strictly specified so that additional buffers are needed to synchronize the delay. Meanwhile, to maintain the symmetry layout of gates and reduce the undesired parasitic magnetic coupling, the AQFP cell library adopts the minimalist design method in which splitters are employed for the gates with multiple fan-outs. Thus, an AQFP circuit may demand numerous splitters and buffers, resulting in a considerable amount of power consumption and delay. This provides a motivation for proposing an effective splitter and buffer insertion algorithm for the AQFP circuits. In this paper, we propose a dynamic programming-based algorithm that provides an optimal splitter and buffer insertion for each wire of the input circuit. Experimental results show that our method is fast, and has a 10% reduction of additional Josephson Junctions (JJs) in the complicated circuits compared with the state-of-the-art method.